K.S.R.M. COLLEGE OF ENGINEERING (UGC-AUTONOMOUS)
Kadapa,Andhra Pradesh, India– 516 003
Approved by AICTE, New Delhi & Affiliated to JNTUA, Ananthapuramu.
An ISO 14001:2004 & 9001: 2015 Certified Institution

Department of ECE

M.Tech Embedded Systems and VLSI Course Structure

Semester-I									
S.No	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	2284101	RTL Simulation and Synthesis With PLDs	PCC	3	0	0	40	60	3
2.	2284102	Microcontrollers and Programmable Digital Signal Processors	PCC	3	0	0	40	60	3
3.	2284103	Research methodology and IPR	-	2	0	0	40	60	2
	Professional Elective Course-I								
4.	2284104 2284105 2284106 2284107	Parallel Processing Digital Signal and Image Processing VLSI Signal Processing Design for testability	PEC	3	0	0	40	60	3
	Professional Elective Course-II								
5.	2284108 2284109 2284110 2284111	Programming Languages for Embedded Systems Micro-Electro Mechanical systems. CAD of Digital System CPLD, FPGA Architectures and Applications.	PEC	3	0	0	40	60	3
6.	2284112	RTL Simulation and Synthesis with PLDs Lab	PCC	0	0	4	50	50	2
7.	2284113	Microcontrollers and Programmable Digital Signal Processors Lab	PCC	0	0	4	50	50	2
8.	2270A02	Disaster Management	AC				40		0
									18

Semester-II									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	2284201	Analog and Digital CMOS VLSI Design	PCC	3	0	0	40	60	3
2.	2284202	Embedded and Real Time Operating Systems	PCC	3	0	0	40	60	3
	Professional Elective Course-III								
3.	2284203 2284204 2284205 2284206	Memory Architectures Advanced Computer Architecture SoC Design Low Power VLSI Design	PEC	3	0	0	40	60	3
	Professional Elective Course-IV								
4.	2284207 2284208 2284209 2284210	Communication Buses and Interfaces Network Security and Cryptography Physical design automation Nano Electronics	PEC	3	0	0	40	60	3
5.	2284211	Analog and Digital CMOS VLSI Design Lab	PCC	0	0	4	50	50	2
6.	2284212	Real Time Operating Systems Lab	PCC	0	0	4	50	50	2
7.	2284213	Technical Seminar	PCC	0	0	4	100	0	2
8.	2270A01	English for Research Paper Writing	AC				40		0
									18

Semester-III									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
		Professional Elective Course-V							
1.	2284301 2284302 2284303 2284304	IOT and its Applications Hardware Software co-design Artificial Intelligence RFIC Design	PEC	3	0	0	40	60	3
		Open Elective Course							
2.	2271305 2271306 2271307 2271308 2271309 2271310	Business Analytics Industrial Safety Operations Research Cost Management of Engineering Projects Composite Materials Waste to Energy	OEC	3	0	0	40	60	3
3.	2284311	Dissertation Phase-I	PR	0	0	20	100	0	10
4	2254312	Co-Curricular activities							2
									18

Semester-IV									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	2284401	Dissertation Phase II	PR	0	0	32	50	50	16
									16

Course Title	RTL SIMULATION AND SYNTHESIS WITH PLDS				M. Tech. ES &VLSI I Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2284101	**PCC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**		

Course Objectives:

- To introduce Verilog HDL for the design and functionality verification of a digital circuit.
- To understand the design of data path and control circuits for sequential machines
- To introduce the concept of realizing a digital circuit using PLDs

Course Outcomes: On successful completion of this course, the students will be able to	
CO 1	Understand the Static Timing Analysis and clock issues in digital circuits
CO 2	Appreciate the analysis of finite state machine of a controlling circuit
CO 3	Develop the Verilog HDL to design a digital circuit.
CO 4	Verify the functionality of the digital designs using PLDs.

UNIT I

Verilog HDL: Importance of HDLs, Lexical Conventions of Verilog HDL Gate level modeling: Built in primitive gates, switches, gate delays Data flow modeling: Continuous and implicit continuous assignment, delays Behavioral modeling: Procedural constructs, Control and repetition Statements, delays, function and tasks.

UNIT II

Digital Design: Design of BCD Adder, State graphs for control circuits, shift and add multiplier, Binary divider. FSM and SM Charts: Finite state diagram, Implementation of sequence detector using FSM, State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier.

UNIT III

ASIC Design Flow: Simulation, simulation types, Synthesis, synthesis methodologies, translation, mapping, optimization, Floor planning, Placement, routing, Clock tree synthesis, Physical verification.

UNIT IV

Static Timing Analysis: Timing paths, Meta-stability, Clock issues, Need and design strategies for multi-clockdomain designs,setup andhold timeViolations, stepsto removeSetup andhold timeviolations.

UNIT V

Digital Design using PLD‟s: ROM, PLA, PAL- Registered PAL‟s, Configurable PAL‟s, GAL. CPLDs: Features, Programming and Applications using Complex Programmable logic devices. FPGAs: Field Programmable gate arrays Logic blocks, routing architecture, design flow.

TEXTBOOKS:

1. Samir Palnitkar, “Verilog HDL, A Guide to Digital Design and Synthesis”, 2nd Edition, 2003.
2. Charles H.Roth, “Fundamentals of Logic Design”, Cengage Learning, 5th Edition, 2010.
3. Bhasker J, “Verilog HDL Synthesis A Practical Primer”, 1st edition, 1998.

REFERENCES:

1. Donald D Givone, “Digital Principles and Design”, TMH, 2016
2. Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books,2002.
3. Richard S. Sandige,“Modern Digital Design”, MGH, International Edition,1990

Course Title	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS				M. Tech. ES &VLSI I Sem			
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
2284102	**PCC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**			

Course Objectives:

- To understand, compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
- To be able to identify and characterize architecture of Programmable DSP Processors.
- To develop small applications by utilizing the ARM processor core and DSP processor based platform.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
CO 2	Identify and characterize architecture of Programmable DSP Processors
CO 3	Develop small applications by utilizing the ARM processor core and DSP processor based platform.

UNIT I

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT II

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration.

UNIT III

LPC 17xx Microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT IV

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.

UNIT V

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for application development for digital signal processing.

TEXT BOOKS:

1. Joseph Yiu, “The definitive guide to ARM Cortex - M3”, Elsevier, 2nd Edition.
2. Venkatramani B. and Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications”, TMH, 2nd Edition
3. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication

REFERENCE BOOKS:

1. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
2. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
3. Technical References and user manuals on www.arm.com.

Course Title	RESEARCH METHODOLOGY AND IPR				M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
2284103	PCC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		2	0	--	2	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understandresearchproblemformulation.
- To Analyzeresearch relatedinformation
- To Followresearchethics
- To understanding that when IPR would take such important place in growth of individuals &nation,it is needless to emphasis the need of information about Intellectual Property Right to bepromotedamongstudents in general&engineeringin particular.
- To understand that IPR protection provides an incentive to inventors for further research work andinvestment in R & D, which leads to creation of new and better products, and in turn brings about,economic growth and social benefits.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand research problem formulation.
CO 2	Analyze research related information
CO 3	Followresearchethics
CO 4	Apply PatentRights in filing.
CO 5	Describe new developments in IPR.

UNITI

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting are search problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, Analysis, interpretation, Necessary instrumentations.

UNIT II

Effective literature studies approaches, Analysis Plagiarism and Research ethics. Effective technical writing, How to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT III

Nature of Intellectual Property: Patents, Designs, Trade and Copyright, Process of Patenting and Development: Technological research, Innovation, Patenting, Development. International Scenario: International Cooperation on Intellectual Property, Procedure for grants of patents, Patent in gender PCT.

UNITIV

Patent Rights: Scope of Patent Rights, Licensing and transfer of technology, Patent in formation and databases, Geographical Indications.

UNIT V

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research Methodology: An Introduction for Science & Engineering students"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, "Research Methodology: A Step by Step Guide for beginners" , 2nd Edition ,

REFERENCE BOOKS:

1. Mayall, "Industrial Design", Mc Graw Hill,1992.
2. Niebel, "Product Design", Mc Graw Hill, 1974.
3. Asimov,"IntroductiontoDesign",PrenticeHall, 1962.
4. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
5. T. Ramappa, "Intellectual Property Rights Under WTO", S.Chand, 2008

Course Title	PARALLEL PROCESSING					M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
2284104	PEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- Tooverview of the architectures and communication networks employed in parallel computers.
- The course covers the foundations for development of efficient parallel algorithms, including examples from relatively simple numerical problems, sorting, and graph problems.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand parallel processing and pipelining techniques.
CO 2	Identify limitations of different architectures of computer
CO 3	Analysis quantitatively the performance parameters for different architectures
CO 4	Investigate issues related to compilers and instruction set based on type of architectures
CO 5	Develop parallel programming techniques.

UNIT I

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

UNIT II

Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

UNIT III

VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

UNIT IV

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions

UNIT V

Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems Customizing applications on parallel processing platforms

TEXT BOOKS:

1. Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGH International Edition
2. Kai Hwang, “Advanced Computer Architecture”, TMH
3. V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.

REFERENCE BOOKS:

1. William Stallings, “Computer Organization and Architecture, Designing for performance “Prentice Hall, Sixth edition
2. Kai Hwang, Zhiwei Xu, “Scalable Parallel Computing”, MGH
3. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan

Course Title	DIGITAL SIGNAL AND IMAGE PROCESSING				M. Tech. ES & VLSI I Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
2284105	PEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	0	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To study the discrete time signals and system in various domains
- To learn the concepts of design of digital filtering
- To study different image enhancement, Restoration and compression techniques
- To understand image segmentation algorithms

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Analyze discrete-time signals and systems in various domains (i.e.Time, Z and Fourier)
CO 2	Design the digital filters (both IIR and FIR) from the given specifications
CO 3	Analyze the quantization effects in digital filters and understand the basics of image sampling, quantization and image transforms.
CO 4	Understand the concepts of image enhancement, image restoration, image segmentation and Color Image processing
CO 5	Analyze various image compression techniques

UNIT I

Review of Discrete Time signals and systems, Characterization in time, Z and Fourier domain, Fast Fourier Transform using Decimation in Time (DIT) and Decimation in Frequency (DIF) Algorithms.

UNIT II

IIR Digital Filters: Introduction, Analog filter approximations–Butterworth and Chebyshev, Design of IIR Digital filters from analog filters using Impulse Invariance, Bilinear Transformation methods.

FIR Digital Filters: Introduction, Design of FIR Digital Filters using Window Techniques, Frequency Sampling technique, Comparison of IIR & FIR filters.

UNIT III

Analysis Of Finite Word length Effects: The Quantization Process and Errors, Quantization of Fixed-Point Numbers, Quantization of Floating- Point Numbers ,Analysis of Coefficient Quantization effects.

Introduction To Digital Image Processing: Introduction, components in image processing system, Applications of Digital image processing, Image sensing and acquisition, Image sampling, Quantization, Basic Relationships between pixels, Image Transforms: 2D-DFT, DCT, Haar Transform.

UNIT IV

Image Enhancement: Intensity transformation functions, histogram processing, fundamentals of spatial filtering, smoothing spatial filters, sharpening spatial filters, the basics of filtering in the frequency domain, image smoothing using frequency domain filters, Image Sharpening using

frequency domain filters ,Selective filtering.

Image Restoration: Introduction, restoration in the presence of noise only-Spatial Filtering, Periodic Noise Reduction by frequency domain filtering, Linear, Position –Invariant Degradations, Estimating the degradation function, Inverse filtering, Minimum mean square error (Wiener) filtering.
Image Segmentation: Fundamentals, point, line, edge detection, thresholding, and region based segmentation.

UNIT V

Image Compression: Fundamentals, Basic compression methods: Huffman coding, Arithmetic coding, Run-Length coding, Block Transform coding, Predictive coding, Wavelet coding.
Color Image Processing: color fundamentals, color models, pseudo color image processing, basics of full color image processing, color transformations, smoothing and sharpening. Image segmentation based on color, noise in color images, color image compression.

TEXT BOOKS:

1. John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Principles, Algorithms, and Applications, Pearson Education , PHI, 2007.
2. S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition, 2006
3. Rafael C. Gonzalez and Richard E.Woods, "Digital Image Processing", Pearson Education, 2011.

REFERENCE BOOKS:

1. Andreas Antoniou, "Digital Signal Processing", TATA Mc Graw Hill, 2006
2. M H Hayes, "Digital Signal Processing", Schaum"s Outlines, TATA Mc – Graw Hill, 2007.
3. Anil K. Jain, "Fundamentals of Digital Image Processing,", Prentice Hall of India, 2012.

Course Title	VLSI SIGNAL PROCESSING				M. Tech ES & VLSI I Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2284106	**PEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**		

Course Objectives:

- To understand the static, small signal and large signal modeling of MOS Transistor.
- To understand the DSP architectures.
- To understand the operation of design aspects of processors.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Ability to modify the existing or new DSP architectures suitable for VLSI.
CO 2	Understand the concepts of folding and unfolding algorithms and applications.
CO 3	Analyze to implement fast convolution algorithms.
CO 4	Develop Low power design aspects of processors for signal processing and wireless applications.

UNIT I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel ProcessingIntroduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT II

Folding and Unfolding: Folding - Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems.
Unfolding - Introduction, An Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT IV

Fast Convolution: Introduction, Cook, Toom Algorithm, Winograd algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution algorithm by Inspection

UNIT V

Digital lattice filter structures, Bit level arithmetic, Architecture, Redundant arithmetic. Numerical Strength reduction, Synchronous wave and asynchronous pipe lines, Low power design. Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

TEXT BOOKS:

1. Keshab K. Parhi , “VLSI Digital Signal Processing Systems, Design and Implementation”, Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, “Analog VLSI Signal and Information Processing”, McGraw Hill, 1994.

REFERENCE BOOKS:

1. S. Y. Kung, H. J. White House, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1985.
2. Jose E. France, Yannis Tsividls, “Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing”, Prentice Hall, 1994.

Course Title	DESIGN FOR TESTABILITY				M. Tech. ES &VLSI			
Course Code	Category	Hours/Week			Credits	Maximum Marks		
2284107	PEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- Toanalyze the digital circuits with the presence of faults.
- To generate the test patterns.
- To understand the concept of controllability and observability.
- To determine the built in self test.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Design digital circuits including various levels of modeling and different approaches for simulation.
CO 2	Analyze the digital circuits with the presence of faults and evaluation of given test set for fault coverage.
CO 3	Create test patterns for detecting single stuck faults in combinational and sequential circuits.
CO 4	Describe controllability and observability and schemes for introducing testability into digital circuits which will make circuits more testable with ease and improve fault coverage.
CO 5	Determine built in self test (BIST) and different approaches for introducing BIST into logic circuits memories and embedded cores.

UNIT I

Introduction to Test and Design for Testability (DFT) Fundamentals. Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of modeling. Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

UNIT II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits.

UNIT III

Testing for single stuck faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models.Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT IV

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT – V

Built-in self-test (BIST) – BIST Concepts and test pattern generation.Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level. Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, embedded memory testing model. Memory test requirements for MBIST.Brief ideas on embedded core testing.

TEXT BOOKS:

1. Miron A bramovici, Melvin A. Breur, Arthur D. Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 2001.
2. Alfred Crouch., "Design for Test for Digital ICs & Embedded Core Systems", Prentice Hall.

REFERENCE BOOKS:

1. Robert J. Feugate, Jr., Steven M. Mentyn, "Introduction to VLSI Testing", Prentice Hall, Englehood Cliffs, 1998.
2. Fault Tolerant & Fault Testable Hardware Design- Parag K. Lala, PHI, 1984

Course Title	PROGRAMMING LANGUAGES FOR EMBEDDED SYSTEM				M. Tech. ES &VLSI I Sem			
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
2284108	**PEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**			

Course Objectives:

- To explore the difference between general purpose programming languages and Embedded Programming Language.
- To provide case studies for programming in embedded systems.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the basics of Embedded C with reference to 8051.
CO 2	Understand how to handle control and data pins at hardware level.
CO 3	Capable of introducing into objective nature of Embedded C.
CO 4	Understand the specifications of real time embedded programming with case studies

UNIT I

Programming Embedded Systems in C Introduction, What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family

Introduction, What‟s in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT II

Reading Switches Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT III

Adding Structure to your Code Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the „Hello Embedded World‟ example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT IV

Meeting Real-Time Constraints Introduction, Creating „hardware delays‟ using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for „timeout‟ mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT V

Case Study: Intruder Alarm System Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

1. Michael J. Pont “Embedded C”, A Pearson Education
2. Mazidi, “PIC Microcontroller and Embedded Systems: Using assembly and C for PIC 18.

REFERENCE BOOKS:

1. Mazidi, “The 8051 Microcontroller and Embedded Systems: Using Assembly and C”.
2. Michael Barr, “Programming Embedded Systems in C & C++”.

Course Title	MICRO-ELECTRO MECHANICAL SYSTEMS.				M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
2284109	PEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	0	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- Able to know a new and upcoming interdisciplinary area.
- To understand generating better electronic gadgets
- Able to know technologies involving miniaturized Electrical, Mechanical and Electro-mechanical devices
- To understand a new stream of Electronics-MEMTRONICS.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	A new and upcoming interdisciplinary area.
CO 2	Generating better electronic gadgets
CO 3	Technologies involving miniaturized Electrical, Mechanical and Electro-mechanical devices
CO 4	A new stream of Electronics-MEMTRONICS

UNIT I

Introduction, Basic Structures of MEM Devices – (Canti Levers, Fixed Beams diaphragms). Broad Response of MEMS to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic stimuli, Compatibility of MEMS with VLSI Applications in Electronics, Broad Advantages and Disadvantages of MEMS from the point of Power Dissipation, Leakage etc.

UNIT II

Review of Mechanical Concepts like Stress, Strain, Bending Moment, and Deflection Curve. Differential equations describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed beam. Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes. Deflection with voltage in C.L, Deflection Vs Voltage Curve, Critical Deflection, Description of the above w.r.t. Fixed Beams. Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions – Transient Response of the MEMS.

UNIT III

Two Terminal MEMS – capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors.Two Terminal MEM Structures. Three Terminal MEM structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications.

UNIT IV

MEM Circuits & Structures for Simple GATES – AND, OR, NAND, NOR, Exclusive OR, simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converters.

Applications for Analog Circuits like Frequency Converters, Wave Shaping. RF Switches for Modulation. MEM Transducers for Pressure, Force Temperature.Optical MEMS.

UNIT V

MEM Technologies: Silicon Based MEMS – Process Flow – Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers etc., Etching Technologies. Metal Based MEMS: Thin and Thick Film Technologies for MEMS. PROCESS flow and Description of the Processes.Status of MEMS in the Current Electronics scenario.

TEXT BOOKS:

1. Gabriel. M. Reviez, R.F. "MEMS Theory", Design and Technology", Jhon Wiley & Sons, 2003.
2. Thimo Shenko, "Strength of Materials", CBS Publishers & Distributors.
3. K. Pitt, M.R. Haskard, "Thick Film Technology and Applications", 1997.

REFERENCE BOOKS:

1. Wise K.D. (Guest Editor), "Special Issue of Proceedings of IEEE", Vol.86, No.8, Aug 1998.
2. Ristic L. (Ed.) Sensor Technology and Devices, Artech House, London 1994

Course Title	CAD OF DIGITAL SYSTEMS.				M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
2284110	PEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	0	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand the fundamentals of CAD tools for modeling, design, test and verification of VLSI Systems.
- To study various phases of CAD, including simulation, physical design, test andVerification.
- To be able to demonstrate the knowledge of computational algorithms and tools for CAD.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Fundamentals of CAD tools for modeling, design, test and verification of VLSI systems.
CO 2	Understand various phases of CAD, including simulation, physical design, test andverification.
CO 3	Demonstrate knowledge of computational algorithms and tools for CAD.

UNIT I

Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules Layout of Basic Devices, Fabrication Process and its Impact on Physical Design, Scaling Methods, Status ofFabricationProcess, Issues related to the Fabrication Process, Future of Fabrication Process, Solutions for Interconnect Issues, Tools for Process Development.

UNIT II

VLSI design automation tools – Data Structures and Basic Algorithms, Basic Terminology, Complexity Issues and NP-hardness , Basic Algorithms, Basic Data Structures, Graph theory and Computational complexity, Tractable and intractable problems.

UNIT III

General purpose methods for combinational optimization – Partitioning- Problem Formulation ,Classification of Partitioning Algorithms, Group Migration Algorithms , Simulated Annealing Simulated Evolution, Other Partitioning Algorithms Performance Driven Partitioning Floor planning- Chip planning, Pin Assignment , Integrated Approach, Placement- Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms , Partitioning Based Placement Algorithms, Performance Driven Placement, Routing -Global Routing,Problem Formulation,Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms. Steiner Tree based Algorithms Integer Programming Based Approach, Performance Driven Routing.

UNIT IV

Simulation- Gate- level Modelling and Simulation, Switch-level Modeling and Simulation, Logic Synthesis and Verification - Introduction to Combinational Logic Synthesis , Binary-decision Diagrams, Two-level Logic Synthesis, High-level Synthesis- Hardware Models for High level

Synthesis , Internal Representation of the Input Algorithm , Allocation, Assignment and Scheduling.

UNIT V

MCMs-VHDL-Verilog-implementation of adders, Subtractors, Multiplexers, Demultiplexers and counters using VHDL.

TEXT BOOKS:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation".

2. S.H. Gerez, "Algorithms for VLSI Design Automation".

REFERENCE BOOKS:

1. S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis"

2. Navabi, "VHDL Analysis & Modeling of digital systems"

Course Title	CPLD, FPGA ARCHITECTURS AND APPLICATIONS.				M. Tech. ES & VLSI I Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2284111	**PEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	0	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**			

Course Objectives:

- Implement given task using FPGA
- Develop test pattern to test the FPGA
- Design a product level approach utilizing FPGAs.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Differentiate between ROM,PAL,PLA,SPLD,CPLD,FPGA
CO 2	Compare the features of Various CPLDs interms of their architecture, Logic blocks
CO 3	Compare the features of Various FPGAs interms of their Architecture, Configurable logic block and routing.
CO4	Gain knowledge on routing algorithms adopted in FPGAs.
CO5	Test a particular PLD using various techniques like design validation, Timing verification.

UNIT I

Programmable logic: Programmable read only memory (prom), Programmable Logic Array (PLA), Programmable Array Logic (PAL). Sequential Programmable Logic Devices (SPLDs).Programmable Gate Arrays (PGAs), CPLD and FPGA, design flow using FPGA, programming technologies.

UNIT II

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA's- XILINX XC4000, Virtex-II FPGA's, XILINX SPARTAN II, Alteras Act1, Act2, Act3 FPGA's, Actel FPGA's, AMD FPGA.

UNITIII

CPLD's: complex programmable logic devices, logic block, I/O block, interconnect matrix, logicblocks and features of Altera flex logic 10000 series CPLD's , max 7000 series CPLD's, AT & T – ORCA's (Optimized Reconfigurable Cell Array), Cypres flash 370 device technology, lattice PLSI's architectures.

UNIT IV

Placement: objectives, placement algorithms**:** Mincut-Based placement, iterative improvement placement, simulatedannealing.Routing: objectives, segmented channel routing, Maze routing, Routability estimation, Net delays, computing signal delay in RC tree networks.

UNIT V

Digital Front End and back End tools for FPGAs & ASICs, FPGA implementation steps .Verification: introduction, logic simulation, design validation, timing verification .Testing

concepts: failures, mechanisms and faults, fault coverage, ATPG methods, and programmability failures.

TEXTBOOKS:

1. P.K. Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Pearson Education 2009.
2. S. Trimberger, Edr, "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.

References:

1. Old Field, R. Dorf, "Field Programmable Gate Arrays", John Wiley & Sons, New york, 1995.
2. Brown, R. Francis, J. Rose, Z. Vransic, "Field Programmable Gate array", Kluwer Publn, 1992.
3. Manuals from Xilinx, Altera, AMD, Actel.

Course Title	RTL SIMULATION AND SYNTHESIS WITH PLDS LAB				M. Tech. ES &VLSI I Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2284112	**PCC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		--	--	4	2	50	50	100
						End Exam Duration: 3Hrs		

Course Objectives:

- To implement the Verilog code for combinational and sequential circuits.
- To implement the Verilog code for Discrete Fourier Transform/FFT algorithm
- To design FSM, Vending Machine.

Course Outcomes: On successful completion of this course, the students will be able to	
CO 1	To design various combinational and sequential circuits.
CO 2	To design FSM machines, Vending machines.
CO 3	Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
CO 4	Realize single port SRAM in Verilog
CO 5	Implement UART/USART in Verilog.

LISTOFEXPERIMENTS:

1. Verilog implementation of 8:1 Mux/Demux,
2. Verilog implementation of Full Adder, 8-bit Magnitude comparator.
3. Verilog implementation of 3-bit Synchronous Counters.
4. Verilog implementation of Parity generator.
5. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
6. Vending machines - Traffic Light controller, ATM, elevator control.
7. PCI Bus & arbiter and downloading on FPGA.
8. UART/ USART implementation in Verilog.
9. Realization of single port SRAM in Verilog.
10. Verilog implementation of Arithmetic circuits like serial adder/ subtractor.
11. Verilog implementation of paralleladder/subtractor, serial/parallel multiplier.
12. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

<table>
<tr><td>Course Title</td><td colspan="5">MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB</td><td colspan="3">M. Tech. ES & VLSI I Sem</td></tr>
<tr><td>Course Code</td><td>Category</td><td colspan="3">Hours/Week</td><td>Credits</td><td colspan="3">Maximum Marks</td></tr>
<tr><td rowspan="2">2284113</td><td rowspan="2">PCC</td><td>L</td><td>T</td><td>P</td><td>C</td><td>Continuous Internal Assessment</td><td>End Exams</td><td>Total</td></tr>
<tr><td>-</td><td>--</td><td>4</td><td>2</td><td>50</td><td>50</td><td>100</td></tr>
<tr><td colspan="5"></td><td colspan="4">End Exam Duration: 3Hrs</td></tr>
<tr><td colspan="9">Course Objectives:
➢ To understand, compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
➢ To be able to identify and characterize architecture of Programmable DSP Processors
➢ To develop small applications by utilizing the ARM processor core and DSP processor based platform.</td></tr>
<tr><td colspan="9">Course Outcomes: On successful completion of this course, the students will be able to</td></tr>
<tr><td>CO 1</td><td colspan="8">Install, configure and utilize tool sets for developing applications based on ARM processor Core SoC and DSP processor.</td></tr>
<tr><td>CO 2</td><td colspan="8">Develop prototype codes using commonly available on and off chip peripherals on theCortex M3 and DSP development boards.</td></tr>
</table>

LIST OF ASSIGNMENTS:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU Tool chain

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6748 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

Course Title	ANALOG AND DIGITAL CMOS VLSI DESIGN					M. Tech. ES & VLSI II Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
2284201	**PCC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs						**End Exam Duration: 3Hrs**		

Course Objectives:

- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Combinational MOS logic circuits, and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.
- Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
- To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Appreciate the trade-offs involved in analog integrated circuit design.
CO 2	Understand and appreciate the importance of noise and distortion in analog circuits.
CO 3	Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
CO 4	Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS, Alternative CMOS Logics, Estimation of Delay and Power, Adders Design.
CO 5	Solve engineering problems for feasible and optimal solutions in the core area of digital ICs.

Digital CMOS Design:

UNIT I

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their Evaluation, Dynamic behavior, Power consumption.

UNIT II

Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.

Combinational logic: Static CMOS design, Logic effort, Rationed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

UNIT III

Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches,Static SR

flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

Analog CMOS Design

UNIT IV

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gatestage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT V

Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise. Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP.

TEXT BOOKS:

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
3. BehzadRazavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

REFERENCE BOOKS:

1. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
2. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
3. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rd Edition.
4. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

Course Title	EMBEDDED AND REAL TIME OPERATING SYSTEMS					M. Tech. ES & VLSI II Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
2284202	**PCC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	-	--	3	40	60	100
Mid Exam Duration: 2Hrs						**End Exam Duration: 3Hrs**		

Course Objectives:

- The main objective of the course is to get students familiar with the typical problems and constraints that arise when designing and developing embedded systems
- The course will also introduce theoretical and practical solutions to these typical problems that the students are expected to master and be able to apply to realistic case studies.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the fundamental concepts of a embedded system, General Purpose Processors and Embedded RTOS Concepts.
CO 2	Apply embedded system concepts in industry, medicine, and defence.
CO 3	Analyze the embedded design models and Design Technology.
CO 4	Design custom single purpose processors.

UNIT I

Introduction: Embedded systems overview, Design challenge, Processor technology, IC technology, Design technology. RT-Level combinational logic, Sequential logic (RT-Level), Custom single purpose processor design (RT-Level), optimizing custom single purpose processors.

UNIT II

General Purpose Processors: Basic architecture, Operation, Programmer‟s View, Development environment, Application specific Instruction Set processors (ASIPs).

UNIT III

State Machine and Concurrent Process models: Introduction, Models Vs Languages, Finite State Machine with Data path model (FSMD), Using State Machines, Program State Machine (PSM),Concurrent Process Model, Concurrent Processes, Communication among processors, Synchronization among processes, Implementation, Data flow model, Real-time Systems.

UNIT IV

Design Technology: Introduction, Automation-The parallel evolution of complication and synthesis, Logic, RT, Behavioral synthesis, System synthesis and hardware/software codesign, Verification of hardware/software co-simulation, Reuse of intellectual property cores.

UNIT V

Embedded RTOS Concepts: Architecture of the Kernel, Tasks and Task Scheduler, interrupt service routines, Semaphores, Mutex, Mail boxes, Message Queues, Event Registers, Pipes, Signals.

TEXT BOOKS:

1. Frank Vahid, Tony D. Givargis, "Embedded Systems Design - A Unified Hardware/Software Introduction", John Wiley & Sons. Inc.2002.
2. Dr. K.V.K.K. Prasad, "Embedded / Real-Time Systems: Concepts, Design and Programming", Dreamtech Publications.

REFERENCE BOOKS:

1. Raj Kamal, "Introduction to Embedded Systems", TMH, 2002.
2. David E. Simon, "An Embedded Software Primer", 1st Edition, Addison Wesley Professional, 2007.

Course Title	MEMORY ARCHITECTURES				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
2284203	PEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand the architectureanddesignsemiconductor memorycircuitsandsubsystems

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Select architecture and design semiconductor memory circuits and subsystems.
CO 2	Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
CO 3	Analyze the state-of-the-art memory chip design

UNIT I

RandomAccessMemoryTechnologies:

Static Random Access Memories (SRAMs), SRAM Cell Structures, MOSSRAM Architecture, MOSSRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT II

DRAMs, MOS DRAM Cell, Bi CMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory Controllers

UNIT III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT IV

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing

UNIT V

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D&3D), Memory Stacks, Memory Testing and Reliability Issues.

TEXTBOOKS:

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience
2. Kiyoo Itoh, "VLSI Memory Chip Design",Springer International Edition

REFERENCEBOOKS:

1. Ashok K Sharma, "SemiconductorMemories:Technology, Testing and Reliability", PHI
2. Luecke Mize Care, "Semiconductor Memory design & application"
3. Belty Prince, "Semiconductor Memory", Design Handbook.

Course Title	ADVANCED COMPUTER ARCHITECTURE				M. Tech. ES & VLSI II Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2284204	**PEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**			

- To Understand the advanced concepts related to computer architecture and storage systems, parallelism and pipelining concepts, the design aspects and challenges

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the advanced concepts related to computer architecture and storage systems.
CO 2	Understand parallelism and pipelining concepts, the design aspects and challenges.
CO 3	Analyze the high performance scalable Multithreaded and multiprocessor systems.

UNIT I

Fundamentals of Computer Design: Technology trends, cost- measuring and reporting performancequantitative principles of computer design.

Instruction Set Principles and Examples: **c**lassifying instruction set- memory addressing- type and sizeof operands- addressing modes for signal processing operations in the instruction set, instructions for control flow, encoding an instruction set, the role of compiler

UNIT II

Instruction Level Parallelism (ILP): overcoming data hazards reducing branch costs, high performanceinstruction delivery, hardware based speculation, limitation of ILP

ILP Software Approach:compiler techniques- static branch protection, VLIW approach, H.W support formore ILP at compile time- H.W verses S.W solutions

UNIT III

Memory Hierarchy Design:cache performance, reducing cache misses penalty and miss rate, virtualmemory, protection and examples of VM.

UNIT IV

Multiprocessors and Thread Level Parallelism:Symmetric shared memory architectures, distributedshared memory, Synchronization, multi threading.

UNIT V

Storage Systems-Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/Osystem.

Interconnection Networks and Clusters:Interconnection network media, practical issues ininterconnecting networks- examples, clusters, designing a Cluster

TEXT BOOKS:

1. John L. Hennessy & David A. Patterson, " Computer Architecture A quantitative approach", 3rd edition, Morgan Kuf mann (An Imprint of Elsevier)
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architectures", Pearson.

REFERENCE BOOKS:

1. Kai Hwang and A. Briggs "Computer Architecture and parallel Processing", International Edition Mc Graw - Hill.
2. Kai Hwang, "Advanced Computer Architecture", McGraw Hill Education,1993.

Course Title	SOC DESIGN					M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
2284205	PEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- The Objective of this course is to provide the students with knowledge about the system architecture and components.
- To understand the SoC process and its memory design

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Identify and formulate a given problem in the frame work of SoC based design approaches for engineering applications
CO 2	Realize impact of SoC on electronic design philosophy and Macro-electronics there by incline towards entrepreneurship & skill development
CO 3	Computedifferent simulation models
CO 4	Analyze the power optimization for digital systems
CO 5	Understand the importance of synthesis

UNITI

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NIS C approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT II

NISC: NISC Control Words methodology, NISC Applications and Advantages, ArchitectureDescription Languages (ADL) for design and verification of Application Specific Instruction setProcessors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISCarchitectures and systems, use of Generic Netlist Representation - A formal language forspecification,compilation and synthesis of embedded processors.

UNIT III

Simulation: Different simulation modes, behavioral, functional, static timing, gate level, switch level,transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems,SoCrelatedmodelingofdatapathdesignandcontrollogic,Minimizationofinterconnectsimpact, clocktreedesign issues.

UNITIV

Low power SoC design/Digital system: Design synergy, Low power system perspective-power gating, clock gating, and adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, powerconsumptionverification.

UNIT V

Synthesis Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXT BOOKS:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.

2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006

REFERENCE BOOKS:

1. Rochit Rajsuman,"System-on-a-chip:Design and test",Advantest America R&D Center, 2000
2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne L uk, "Computer System Design: System – on - Chip". Wiley

Course Title	LOW POWER VLSI DESIGN				M. Tech. ES & VLSI IISem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
2284206	PEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- Study different abstraction levels in VLSI Design and the impact of power reduction methods at higher levels
- Apply leakage control mechanisms to reduce static power consumption in DSM VLSI regime
- Apply technology independent and technology-dependent techniques for Dynamic power reduction in CMOS circuits
- Study and apply various software power estimation and optimization techniques for low power VLSI system design
- Apply low power circuit and architectural techniques for reducing power consumption in SRAM designs

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	**Distinguish** the impact of various power reduction techniques at different levels of VLSI Design
CO 2	**Identify** the sources of power dissipation and apply leakage control techniques to reduce static power consumption in CMOS circuits
CO 3	**Apply** technology independent and technology-dependent techniques for Dynamic power reduction in CMOS circuits
CO 4	**Analyze** different power reduction techniques for VLSI systems at Design time, Run-time and Stand-by modes
CO 5	**Employ** software power estimation and optimization methods for low power VLSI system design

UNIT I

Introduction to Low Power design: SOC levels, Emerging zero-power applications (WSN), Design-productivity challenge, Impact of implementation choices, Motivation for LPD, Basic VLSI Design Flow, Optimization examples at various levels (System, Sub-system, RTL, Gate, Circuit and Device levels). Sources of power dissipation, MOS transistor leakage components, Static Power dissipation, Active Power dissipation, Circuit Techniques for Low Power Design

UNIT II

Power Optimization Techniques – I: Dynamic Power Reduction Approaches, Circuit Parallelization, Voltage Scaling Based Circuit Techniques, Circuit Technology – Independent Power Reduction, Circuit Technology Dependent Power Reduction; Leakage Power Reduction – Leakage Components, Design Time Reduction Techniques, Run-time Stand-by Reduction Techniques, Run-time Active Reduction Techniques Reduction in Cache Memories.

UNIT III

Power Optimization Techniques – II**:** Low Power Very Fast Dynamic Logic Circuits, Low Power Arithmetic Operators, Energy Recovery Circuit Design, Adiabatic – Charging Principle and its implementation issues.

Software Design for Low Power**:** Sources of Software Power Dissipation, Software Power Estimation, Software Power Optimizations, Automated Low-Power Code Generation, Co-design for Low Power.

UNIT IV

Low Voltage Low Power Static Random Access memories: Basics, Race between 6T and 4T memory cells, LVLP SRAM Cell designs- Shared bit-line SRAM cell configuration, Power efficient 7T SRAM cell with current mode read and write, The 1T SRAM cell, Pre-charge and Equalization Circuit, Dynamic and static decoders, Voltage Sense amplifier, Output Latch,

Low Power SRAM Techniques: Sources of SRAM Power, Low Power Circuit techniques such as capacitance reduction, Leakage current reduction.

UNIT V

Large LP VLSI System design and Applications: Architecture-driven Voltage Scaling, Power optimization using operation reduction and operation substitution, Pre-computation based optimization, Multiple and Dynamic supply voltage design, Choice of supply voltages, varying the clock speed, varying the VDD of RAM structures, Gated Clocking. Leakage current reduction in medical devices (Ref-1)

TEXT BOOKS:

1. Kiat - Seng Yeo and Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems, Tata Mc Graw hill Edition, 2005. (Units I, IV and V)
2. Christian Piguet, "Low Power CMOS Circuits Technology, Logic Design and CAD Tools", 1st Indian Reprint, CRC Press, 2010.(Units II and III)
3. Kaushik Roy and Sharat Prasad, " Low-Power CMOS VLSI Circuit Design" , Wiley Pub., 2000 (Unit III)

REFERENCE BOOKS:

1. DimitriosSoudris, Christian Piguet and CoastasGoutis, "Designing CMOS Circuits for Low Power", Kluwer Academic Pub, 2002
2. J. Rabaey, Low Power Design Essentials, 1st Edition, Springer Publications, 2010

Course Title	COMMUNICATION BUSES AND INTERFACES				M. Tech. ES & VLSI II Sem			
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
22584207	**PEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**			

Course Objectives:

- To DevelopAPIsforconfiguration,readingandwritingdataontoserialbus.
- To learn how to selectaparticularserialbussuitableforaparticularapplication

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Selectaparticularserialbussuitableforaparticularapplication.
CO 2	DevelopAPIsforconfiguration,readingandwritingdataontoserialbus.
CO 3	Designanddevelopperipherals thatcanbeinterfaced todesiredserialbus.

UNITI

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate,featuresLimitations andapplications ofRS232, RS485,I^2C , SPN

UNIT II

Architecture-ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Objectlayer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ackslot, Inter frame spacing, Bit spacing, Applications.

UNIT III

Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration,Hardwareand Softwareimplementation, Hardwareprotocols, Applications.

UNIT IV

Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, isochronous transfer. Enumeration-Device detection, Default state, addressed state, Configured state, enumeration sequencing. Descriptortypesandcontents-Devicedescriptor,configurationdescriptor, Interfacedescriptor,Endpointdescriptor,Stringdescriptor.Devicedriver.

UNIT V

DatastreamingSerialCommunicationProtocol-

SerialFrontPanelDataPort(SFPDP)configurations,Flowcontrol, serial FPDPtransmission frames, fiberframes andcopper cable.

TEXT BOOKS

1. Wilfried Voss, "A Comprehensive Guide to controller Area Network", Copper hill Media Corporation, 2nd Ed., 2005.
2 Jan Axelson, "Serial Port Complete-COM Ports, USB Virtual Com Ports and Ports for Embedded systems-, Lakeview Research, 2nd Ed.,

REFERENCE BOOKS

1. Jan Axelson, "USB Complete", Penram Publications.
2 PCI Express Technology– Mike Jackson, Ravi Budruk, Mind share Press

Course Title	NETWORK SECURITY AND CRYPTOGRAPHY				M. Tech. ES & VLSI II Sem			
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
		L	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
2284208	**PEC**	3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**			

Course Objectives:

- To understand the security & number theory
- To learn about Key Distribution and Management, Diffie-Hellman Key Exchange

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Identifyand utilizedifferent formsof cryptographytechniques.
CO 2	Incorporateauthenticationandsecurityinthenetworkapplications.
CO 3	Distinguishamongdifferenttypes ofthreatsto the systemand handlethesame

UNITI

Security&NumberTheory: Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptan alysis of Classical Encryption Techniques. Introduction, Fermat‟s and Euler‟s Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT II

Private-Key(Symmetric)Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Crypt analysis.

UNIT III

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD -160, HMAC.

UNIT IV

Authentication: IP and Web Security Digital Signatures, Digital Signature Standards,

Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key

Management, WebSecurity Considerations, Secure Socket Layer and Transport Layer Security,

Secure ElectronicTransaction.

UNIT V

System Security: Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans,

Virus Counter measures, Firewalls, Firewall Design Principles, Trusted Systems.

TEXTBOOKS:

1. William Stallings, “Cryptography and Network Security, Principles and Practices”, Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, “Network Security, Private Communicationina Public World”, PrenticeHall, 2ndEdition

REFERENCEBOOKS:

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, “Security Architecture, Design Deployment and Operations”, RSA Press,
2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, “InsideNetworkPerimeter Security”, Pearson Education,2ndEdition
3. Richard Bejtlich, “The Practice of Network Security Monitoring: Understanding Incident Detection and Response”, William Pollock Publisher, 2013

Course Title	PHYSICAL DESIGN AUTOMATION				M. Tech. ES & VLSI II Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2284209	**PEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**		

Course Objectives:

- To Understand the relationship between design automation algorithms and Various constraints posed by VLSI fabrication and design technology
- To Identify layout optimization techniques and map the algorithms

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the relationship between design automation algorithms and Various constraints posed by VLSI fabrication and design technology.
CO 2	Adapt the design algorithms to meet the critical design parameters.
CO 3	Identify layout optimization techniques and map the algorithms
CO 4	Developproto-typeEDAtoolandtest itsefficacy

UNITI

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and AdditionalFabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi-chip modules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

UNITII

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms

UNITIII

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbor pointers, corner stitching, multi-layer operations.

UNITIV

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum colouring, maximum k-independent set algorithm, algorithms forcirclegraphs.

UNIT V

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms

TEXTBOOKS:

1. Naveed Shervani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapat nekar, “Handbook of Algorithms for Physical Design Automation”, CRC Press,2008.

REFERENCE BOOKS:

1. Sarrafzadeh, M. and Wong, C.K, “An Introduction to VLSI Physical Design”, 4th Edition, McGraw-Hill
2. Wolf. W, “Modern VLSI Design System on Silicon”, 2nd Ed., Pearson Education.
3. Dreschler, “Evolutionary Algorithms for VLSI CAD”, 3rd Edition, Springer.

Course Title	NANO ELECTRONICS					M. Tech. ES & VLSI II Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
2284210	**PEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**			

Course Objectives:

- To study the basics of electronics, transistors.
- To Understand the band structure models
- To Understand the nanocapacitors, coulomb blockade

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	To know nanoelectronics holds the capacity for mass production of high-quality nanodevices with an enormous variety of applications
CO 2	Design the scaling of transistors
CO 3	Analyze the molecular electronics or revolutionary engineering solutions
CO 4	Analyze the Electron transport in semiconductors and nanostructures
CO 5	Design Single modulation-doped heterojunctions

UNIT I

Free Electron Theory & The New Ohm‟s Law: Why Electrons flow, Classical free electron theory, Somerfield‟s theory, The quantum of conductance, Coulomb blockade, Towards Ohm‟s law. The Elastic Resistor: Conductance of an Elastic Resistor, Elastic Resistor- Heat dissipation.

UNIT II

Materials for nanoelectronics: Semiconductors, Crystal lattices: bonding in crystals, Electron energy bands, Semiconductor hetero structures, Lattice - matched and pseudo morphic hetero structures, Inorganic nanowires, Organic semiconductors, Carbon nano materials: nanotubes and fullerenes.

UNIT III

Ballistic and Diffusive Transport: Ballistic and Diffusive Transfer Times, Channels for Conduction Conductivity, Conductivity: E(p) or E(k) Relations, Counting States, Drude Formula, Quantized Conductance, Electron Density –Conductivity.

UNIT IV

Electron transport in semiconductors and nanostructures: Time and length scales of the electrons in solids, Statistics of the electrons in solids and nanostructures, Fermi statistics for electrons, the density of states of electrons in nanostructures, Electron transport in nanostructures.

UNIT V

Electrons in traditional low-dimensional structures: Electrons in quantum wells: Single modulation-doped heterojunctions, Numerical analysis of a single heterojunction, Control of charge transfer, Electrons in quantum wires, Electron transport in quantum wires, Electrons in quantum dots.

TEXT BOOKS:

1. Introduction to Nano Science and Technology by S.M. Lindsay.
2. Supriyo Dutta, "Lessons from Nano science: A Lecture Note Series", World Scientific (2012).

REFERENCE BOOKS:

1. Supriyo Dutta – "Quantum Transport- Atom to Transistor", Cambridge University Press (2005).
2. Vladimir.V. Mitin, "Introduction to Nano electronics: Science, Nanotechnology, Engineering & Applications"

Course Title	ANALOG AND DIGITAL CMOS VLSI DESIGN LAB				M. Tech. ES & VLSI II Sem			
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
2284211	**PCC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		--	--	4	2	50	50	100
					End Exam Duration: 3Hrs			

Course Objectives:

- To learn Physical Design i.e. Stick diagrams, Lambda Design Rules and Layout making of VLSI circuits.
- To provide students with an opportunity to practice on various softwares & tools for VLSI Design and develop the mos transistors.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Write HDL code for basic as well as advanced digital integrated circuits.
CO 2	Import the logic modules into FPGA Boards.
CO 3	Synthesize Place and Route the digital ICs.
CO 4	Design, Simulate and Extract the layouts of Analog IC Blocks using EDA tools.

LIST OF MAJOR EQUIPMENTS & SOFTWARE

1. FPGA Kits with
2. XILINX Simulator
3. Microwind
4. LT Spice

LIST OF EXPERIMENTS:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. simple current mirror
6. cascode current mirror.
7. Wilson current mirror.
8. Full Adder
9. RS-Latch
10. Clock Divider
11. JK-Flip Flop
12. Synchronous Counter
13. Asynchronous Counter
14. Static RAM Cell

Course Title	REAL TIME OPERATING SYSTEM LAB				M. Tech. ES & VLSI II Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2284212	**PCC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		--	--	4	2	50	50	100
						End Exam Duration: 3Hrs		

Course Objectives:

- Able to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand an application that creates two tasks that wait on a timer whilst the main task loops
CO 2	Analyze how to write an application to Test message queues and memory blocks
CO 3	Design & Develop an image processing application with Linux OS on Xilinx Zynq FPGA

List of Experiments (As per curriculum):

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks.
   b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.
6. Interfacing Programs: Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task to Blinking two different LEDs at different timings
8. Write an application that creates a two task displaying two different messages in LCD display in two lines.
9. Sending messages to mailbox by one task and reading the message from mailbox by another task.
10. Sending message to PC through serial port by three different tasks on priority Basis.
11. Porting Linux and developing simple application on Xilinx Zed board
12. Developing image processing application with Linux OS on Xilinx Zynq FPGA

List of Experiments (Beyond the Syllabus):

1. Simulating a stepper-motor driver
2. Write simple applications using RTX (ARM Keil‟s real time operating system, RTOS)

Course Title	IOT AND IT'S APPLICATIONS					M. Tech. ES & VLSI III Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
2284301	**PEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**			

Course Objectives:

- To understand the fundamentals of IOTTechnologies.
- To learn different IOT protocols & IT access technologies

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	ApplytheKnowledgeinIOTTechnologies andDatamanagement.
CO 2	Determinethevalueschains PerspectiveofM2M toIOT.
CO 3	ImplementthestateoftheArchitectureof anIOT.
CO 4	CompareIOTApplicationsin Industrial &realworld.
CO 5	Demonstrateknowledge andunderstandingthesecurityandethicalissues ofanIOT.

UNIT I

FUNDAMENTALS OF IoT- Evolution of Internet of Things, Enabling Technologies, IoTArchitectures,oneM2M,IoTWorldForum(IoTWF)andAlternativeIoTmodels,SimplifiedIoTArchitecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoTecosystem,Sensors, Actuators, Smart ObjectsandConnectingSmart Objects.

IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARMCortex Processors, Arduino andIntel Galileo boards.

UNIT II

IoT PROTOCOLS- IT Access Technologies: Physical and MAC layers, topology and Securityof IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions,Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routingover Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: Co AP and MQTT

UNITIII

DESIGNANDDEVELOPMENT-Design Methodology, Embedded computing logic, Microcontroller, Systemon Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming

UNIT IV

DATA ANALYTICS AND SUPPORTING SERVICES- Structured Vs Unstructured Data and Datain Motion Vs Datain Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, XivelyCloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management withNETCONF-YANG

UNIT V

CASE STUDIES / INDUSTRIAL APPLICATIONS: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts.

Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi/Intel Galileo/ARM Cortex/ Arduino)

TEXTBOOKS:

1. David Hanes, Gonzalo Salgueiro, Patrick Gross etete, Rob Barton and Jerome Henry, "IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things", Cisco Press, 2017.

2. A rshdeep Bahga, Vijay Madisetti "Internet of Things - A hands - on approach", Universities Press, 2015

REFERENCE BOOKS:

1. Olivier Hersent, David Boswarthick, Omar Elloumiand Wiley "The Internet of Things – Key applications and Protocols", 2012 (forUnit 2).
2. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyleand, "From Machine – to – Machine to the Internet of Things –Introduction to a New Age of Intelligence", Elsevier, 2014.

Course Title	HARDWARE SOFTWARE CO DESIGN				M. Tech. ES & VLSI III Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2284302	**PEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**		

Course Objectives:

- To design and analyze Hardware-Software Code design Methodology
- To Understand the importance of system level specification languages
- To design and compiler development environment

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Explain AbouttheHardware-SoftwareCode design Methodology
CO 2	Analyze how to select a target architecture and how a prototype is built
CO 3	Explain how emulation of a prototype is done.
CO 4	Briefviewaboutcompilationtechnologiesandcompilerdevelopmentenvironment.
CO 5	Understand the importance of system level specification languages and multi-language co-simulation.

UNIT I

Co-Design Issues: Co-Design Models, Architectures, Languages, A Generic Co-design Methodology**.**

Co-Synthesis Algorithms: Hardware software synthesis algorithms, hardware – software partitioning distributed system co-synthesis

UNIT II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures**:** Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP 21060, TMS320C60), Mixed Systems.

UNIT III:

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT IV

Design Specification and Verification: Design, co - design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, Interface verification

UNIT V

Languages for System-Level Specification and Design-I**:** System-level specification, design representation for system level synthesis, system levelspecificationlanguages.Languages for System-Level Specification and Design-II Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system

TEXT BOOKS:

1. Wayne Wolf , "Hardware / Software Co- Design Principles and Practice", Jorgen Staunstrup, 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, "Hardware / Software Co- Design", 2002, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design", 2010, Springer

Course Title	ARTIFICIAL INTELLIGENCE				M. Tech. ES & VLSI III Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
2284303	PEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To Understand the concept of Artificial Intelligence
- To Understanding reasoning and fuzzy logic for artificial intelligence
- To Analyze Symbolic Reasoning Under Uncertainty

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	UnderstandtheconceptofArtificialIntelligence
CO 2	Explain the searchtechniquesandknowledgerepresentationissues
CO 3	Understandingreasoning and fuzzylogic forartificial intelligence
CO 4	Analyze SymbolicReasoningUnderUncertainty
CO 5	Understandinggameplayingandnaturallanguageprocessing

UNIT I

What is AI (Artificial Intelligence)? : The AI Problems, The Underlying Assumption, What are Techniques, The Level Of The Model, Criteria For Success, Some General References, One Final WordProblems, State Space Search & Heuristic Search Techniques: Defining The Problems As A State SpaceSearch, Production Systems, Production Characteristics, Production System Characteristics, And IssuesIn The Design Of Search Programs, Additional Problems. Generate-And-Test, Hill Climbing, Best-FirstSearch,Problem Reduction, Constraint Satisfaction,Means-Ends Analysis.

UNIT II

Knowledge Representation Issues: Representations and Mappings, Approaches To Knowledge Representation. Using Predicate Logic: Representation Simple Facts In Logic, Representing Instance And Isa Relationships, Computable Functions And Predicates, Resolution. Representing Knowledge Using Rules: Procedural versus Declarative Knowledge, Logic Programming, and Forward Versus Backward Reasoning.

UNIT III

Symbolic Reasoning Under Uncertainty: Introduction To Nomonotonic Reasoning, Logics For Non-monotonic Reasoning. Statistical Reasoning: Probability And Bays‟ Theorem, Certainty Factors And Rule-Base Systems, Bayesian Networks, Dempster Shafer Theory, Fuzzy Logic, Weak Slot-and-Filler Structures: Semantic Nets, Frames. Strong Slot-and-Filler Structures: Conceptual Dependency, Scripts, CYC.

UNIT IV

Game Playing: Overview, And Example Domain: Overview, Mini Max, Alpha-Beta Cut-off,

Refinements, Iterative deepening, The Blocks World, Components Of A Planning System, Goal Stack Planning, Nonlinear Planning Using Constraint Posting, Hierarchical Planning, ReactiveSystems, Other Planning Techniques. Understanding: What understands? What makes it hard? As constraint satisfaction

UNIT V

Natural Language Processing: Introduction, Syntactic Processing, Semantic Analysis, SemanticAnalysis, Discourse And Pragmatic Processing, Spell Checking Connectionist Models: Introduction: Hopfield Network, Learning In Neural Network, Application Of Neural Networks,RecurrentNetworks,Distributed Representations,Connectionist AIAnd SymbolicAI

TEXT BOOKS:

1. Elaine Richand Kevin Knight "Artificial Intelligence", 2nd Edition, Tata Mc Graw-Hill, 2005.
2. Stuart Russel and Peter Norvig,"Artificial Intelligence: A Modern Approach", 3rd Edition, Prentice Hall, 2009.

REFERENCE BOOKS:

1. Denis Rothmanl, "Artificial Intelligence" By Example-2nd edition.
2. Vinod Chandra, "Artificial Intelligence and Machine Learning" 1st Edition.

Course Title	RFIC DESIGN					M. Tech. ES & VLSI III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
2284304	PEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To design various constituents‟ blocks of RF receiver front end
- To Understand the design bottlenecks specific to RF IC design
- To Specify noise and interference performance metrics like noise figure

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the design bottlenecks specific to RF IC design, linearity related issues, ISI
CO 2	Identify noise sources, develop noise models for the devices and systems
CO 3	Specify noise and interference performance metrics like noise figure, IIP3 and different matching criteria.
CO 4	Comprehend different multiple access techniques, wireless standards
CO 5	Design various constituents‟ blocks of RF receiver front end

UNIT I

Introduction to RF and Wireless Technology: Complexity Comparison, Design Bottle Necks, Applications, Analog And Digital Systems, Choice of Technology.

UNIT II

Basic Concepts in RF Design**:** Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT III

Multiple Access: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards. TRANSCEIVER ARCHITECTURES: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

UNIT IV

Amplifiers, Mixers and Oscillators: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

UNIT V

Power Amplifiers: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques

TEXT BOOKS:

1. Behzad Razavi, “RF Microelectronics”, Prentice Hall of India, 2001

2. Thomas H. Lee, “The Design of CMOS Radio Integrated Circuits”, Cambridge University Press.

REFERENCE BOOKS:

1. Jeremy Everard, “Fundamentals of RF Circuit Design with Low Noise Oscillators”,
2. Peter b. Kenington, “High Linearity RF Amplifier Design”,

Course Title	BUSINESS ANALYTICS				M. Tech. ES &VLSI III Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2271305	**OEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**		

Course Objectives:

Understand the role of business analytics within anorganization.

- Analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of anorganization.
- To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decisionmaking.
- To become familiar with processes needed to develop, report, and analyze businessdata.Use decision-making tools/Operations researchtechniques.
- Mange business process using analytical and managementtools.
- Analyze and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospaceetc.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Students will demonstrate knowledge of dataanalytics.
CO 2	Students will demonstrate the ability of think critically in making decisions based on data and deepanalytics.
CO 3	Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support businessdecision-making
CO 4	Students will demonstrate the ability to translate data into clear, actionableinsights.

UNIT I

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modeling, sampling and estimation methods overview.

UNIT II

Trendiness and Regression Analysis: Modeling Relationships and Trends in Data, simple Linear Regression.Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

UNIT III

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes.Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modeling, nonlinear Optimization.

UNIT IV

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model,
Overbooking Model, Cash Budget Model.

UNIT V

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, the Value of Information, Utility and Decision Making. Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Datajournalism.

REFERENCE BOOKS:

1. Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, "Business analytics Principles, Concepts, and Applications", Pearson FT Press.
2. James Evans, "Business Analytics" , Pearsons Education

Course Title	INDUSTRIAL SAFETY				M. Tech. ES &VLSI III Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2271306	**OEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**		

Course Objectives:

- To Understand the Fundamentals of maintenance engineering.
- To Understand the Fire prevention and firefighting, equipment andmethods.
- Analyze the fault tracing-concept and importance.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	To Understand the Fundamentals of maintenance engineering
CO 2	To Understand the Fire prevention and firefighting, equipment andmethods
CO 3	Analyze the fault tracing-concept and importance
CO 4	Analyze the Steps/procedure for periodic and preventive maintenance

UNIT I

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and fire fighting, equipment and methods.

UNIT II

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT III

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT IV

Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic,automotive, thermal and electrical equipment‟s like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internalcombustion engine, v. Boiler,

Electrical motors, Types of faults in machine tools and their generalcauses

UNIT V

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii.Air compressors, iv. Diesel generating (DG) sets Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept andimportance

REFERENCE BOOKS:

1. Higgins & Morrow, "Maintenance Engineering Handbook", Da Information Services.
2. H. P. Garg, "Maintenance Engineering", S. Chand and Company.
3. Audels, "Pump-hydraulic Compressors", Mc graw Hill Publication

Course Title	OPERATION RESEARCH				M. Tech. ES &VLSI III Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2271307	**OEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**		

Course Objectives:

- To understand the dynamic programming to solve problems ofdiscreet andcontinuous variables.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Able to apply the dynamic programming to solve problems of discreet and continuous variables.
CO 2	Able to apply the concept of non-linearprogramming
CO 3	Able to carry out sensitivityanalysis
CO 4	Able to model the real world problem and simulateit

UNIT I

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

UNIT II

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

UNIT III

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

UNIT IV

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

UNIT V

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

REFERENCE BOOKS:

1. H.A. Taha, “Operations Research - An Introduction”, PHI, 2008
2. H.M. Wagner, “Principles of Operations Research”, PHI, Delhi,1982.
3. J.C. Pant, “Introduction to Optimisation: Operations Research”, Jain Brothers, Delhi,2008
4. Hitler Libermann, “Operations Research”, McGraw Hill Pub, 2009
5. Panner Selvam, “Operations Research”, Prentice Hall of India, 2010

Course Title	COST MANAGEMENT OF ENGINEERING PROJECTS				M. Tech. ES &VLSI III Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
		L	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
2271308	**OEC**	3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**			

Course Objectives:

- To understand the Overview of the Strategic Cost Management Process.
- To understand Cost Behavior and Profit Planning Marginal Costing

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	To understand the Overview of the Strategic Cost Management Process
CO 2	Analyze various stages of project execution
CO 3	Evaluate Bar charts and Network diagram

UNIT I

Introduction and Overview of the Strategic Cost Management Process: Cost concepts in decision-making; relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

UNIT II

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non- technical activities.Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts.Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

UNIT III

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems.Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector.

UNIT IV

Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints.Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis.Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets.Measurement of Divisional profitability pricing decisions including transfer pricing.

UNIT V

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

REFERENCE BOOKS:

1. "Cost Accounting A Managerial Emphasis", Prentice Hall of India, NewDelhi
2. Charles T. Horngren and George Foster, "Advanced Management Accounting"
3. Robert S Kaplan, Anthony A. Alkinson, "Management & Cost Accounting"
4. Ashish K. Bhattacharya, "Principles & Practices of Cost Accounting", A. H. Wheeler publisher
5. N.D. Vohra, "Quantitative Techniques in Management", Tata McGraw Hill Book Co. Ltd.

Course Title	COMPOSITE MATERIALS				M. Tech. ES &VLSI III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
2271309	OEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand thecharacteristics of Composite materials
- To understand Manufacturing of Metal Matrix Composites

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	understand theClassification and characteristics of Composite materials
CO 2	Analyze the Manufacturing of Ceramic Matrix Composites
CO 3	Analyze the Manufacturing of Polymer Matrix Composites

UNIT I

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites.Functional requirements of reinforcement and matrix.Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT II

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT III

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostaticpressing.Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT IV

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

UNIT V

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TEXT BOOKS

1. R.W.Cahn , VCH, "Material Science and Technology", Vol 13 , Composites, West Germany.
2. WD Callister, Jr., Adapted by R. Balasubramaniam, "Materials Science and Engineering - An introduction", John Wiley & Sons, NY Indian edition, 2007.

REFERENCE BOOKS:

1. Ed-Lubin, "Hand Book of Composite Materials".
2. K.K.Chawla, "Composite Materials".
3. Deborah D.L. Chung, "Composite Materials Science and Applications".
4. Danial Gay, Suong V. Hoa, and Stephen W. Tasi, "Composite Materials Design and Applications"

Course Title	WASTE TO ENERGY				M. Tech. ES &VLSI III Sem		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**	
2271310	**OEC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**		

Course Objectives:

- To understand theClassification of waste as fuel – Agro based, Forest residueIndustrial waste - MSW – Conversion devices – Incinerators

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the Classification of waste as fuel
CO 2	Explain the Properties of biogas
CO 3	Design and constructional features - Biomass resources and their classification - Biomass conversion processes

UNIT I

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT II

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT III

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT IV

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT-V

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme inIndia.

REFERENCE BOOKS

1. Desai, Ashok V., "Non-Conventional Energy", Wiley Eastern Ltd.,1990.
2. Khandelwal, K. C. and Mahdi, S. S., "Bio gas Technology - A Practical Hand Book", Vol. I & II, Tata McGraw Hill Publishing Co. Ltd.,1983.
3. Challal, D. S., "Food, Feed and Fuel from Biomass", IBH Publishing Co. Pvt. Ltd., 1991.
4. C. Y. Were Ko - Brobby and E. B. Hagan, "Biomass Conversion and Technology", John Wiley & Sons, 1996