KANDULA SRINIVASA REDDY MEMORIAL COLLEGE OF ENGINEERING
(AUTONOMOUS)

KADAPA-516003. AP

(Approved by AICTE, Affiliated to JNTU A, Ananthapuramu, Accredited by NAAC)

(An ISO 9001-2008 Certified Institution)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Certification Course

On

"MSP 430 LaunchPad Programming"

Resource Persons : Dr.G.Hemalatha, Professor Dept. of ECE, KSRMCE

Smt.K.Divyalakshmi, Assistant professor, Dept. of ECE,KSRMCE

Course Coordinators: Dr.G.Hemalatha, Professor Dept. of ECE, KSRMCE

Smt.K.Divyalakshmi, Assistant professor, Dept. of ECE,KSRMCE

Duration : 19/07/2019 to 06/08/2019

K.S.R.M. COLLEGE OF ENGINEERING

(UGC-AUTONOMOUS)

Kadapa, Andhra Pradesh, India– 516 003

Approved by AICTE, New Delhi & Affiliated to JNTUA, Ananthapuramu.

An ISO 14001:2004 & 9001: 2015 Certified Institution

Lr./KSRMCE/ECE/2019-20/ Date:10/07/2019

To
The Principal,
KSRMCE,
Kadapa.

Respected Sir,

Sub: Permission to Conduct Certification Course on "**MSP430 Launchpad programming**" **19/07/2019 to 06/08/2019**–Req- Reg.

The Department of Electronics and communication engineering is planning to offer a Certification Course on "MSP430 Launchpad programming" to B. Tech. students. The course will be conducted from **19/07/2019 to 06/08/2019**. In this regard, I kindly request you to grant permission to conduct a Certification Course.

Thanking you sir,

K Divyalakshmi
Yours faithfully

(Smt.K.Divyalakshmi, Asst.Professor in ECE)

forwarded to the Principal Sir

V.S.S. Murty
PRINCIPAL
K.S.R.M. COLLEGE OF ENGINEERING
KADAPA-516005, (A.P.)

K.S.R.M. COLLEGE OF ENGINEERING

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Kadapa, Andhra Pradesh, India– 516 003

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Cr./KSRMCE/ECE/2019-20/ Date: 12/07/2019

Circular

The Department of Electronics and Communication Engineering is offering a Certification Course on "MSP 430 Launchpad programming" from **19/07/2019 to 06/08/2019** to B.Tech students. In this regard, interested students are requested to register their names for the Certification Course with Course Coordinator.

For further information contact the Course Coordinator.

Course Coordinator: Smt.K.Divyalakshmi, Asst.professor, Dept. of ECE.-KSRMCE.
Contact No: 9494947993

HoD

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
KADAPA - 516 003

Cc to:

IQAC-KSRMCE

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Date:

DEPARTMENT OF ECE

REGISTRATION FORM

Certification Course

On

"MSP 430 Launchpad programming" From 19/07/2019 to 06/08/2019

S.No	Full Name	Roll Number	Branch	Semester	Signature

Coordinators **HoD**

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DEPARTMENT OF ECE

REGISTRATION FORM

Certification Course

On

"MSP 430 Launch pad programming"

From 19/07/2019 to 06/08/2019

S.No	Full Name	Roll Number	Branch	Semester	Signature
1.	Bandi Praneeth	179Y1A0418	ECE	V SEM	
2.	Banthulla Anil Kumar Raju	179Y1A0419	ECE	V SEM	
3.	Basireddy Mahesh Kumar Reddy	179Y1A0420	ECE	V SEM	
4.	Bayyarapu Suresh	179Y1A0422	ECE	V SEM	
5.	Bheemavarapu Vara Lakshmi (W)	179Y1A0423	ECE	V SEM	
6.	Bukkey Rakesh Naik	179Y1A0426	ECE	V SEM	
7.	Chagaleti Surya Narayana Reddy	179Y1A0427	ECE	V SEM	
8.	Chamarthi Sanjeevaraju	179Y1A0428	ECE	V SEM	
9.	Chavva Jaswitha	179Y1A0429	ECE	V SEM	
10.	Chilla Venkateswara Reddy	179Y1A0431	ECE	V SEM	
11.	Dadiboyina Lohitha	179Y1A0433	ECE	V SEM	
12.	Dara Sekhar	179Y1A0435	ECE	V SEM	
13.	Devagudi Venkata Subbaiah	179Y1A0436	ECE	V SEM	
14.	Goparajulu Renuka Harshitha	179Y1A0452	ECE	V SEM	
15.	Gorla Sushmitha Reddy	179Y1A0454	ECE	V SEM	

16.	Guduru Harikrishna	179Y1A0455	ECE	V SEM	
17.	Gundladurthi Balayalla Reddy	179Y1A0456	ECE	V SEM	
18.	Julakalva Niranjanareddy	179Y1A0458	ECE	V SEM	
19.	Kalluru Sunandhana	179Y1A0459	ECE	V SEM	
20.	Kambam Vasu Kalyan Reddy	179Y1A0460	ECE	V SEM	
21.	Kambella Samba	179Y1A0461	ECE	V SEM	
22.	Kanala Pramod Kumar Reddy	179Y1A0463	ECE	V SEM	
23.	Ketha Madhava Reddy	179Y1A0464	ECE	V SEM	
24.	Kollapudi Keerthana	179Y1A0467	ECE	V SEM	
25.	Komme Seshu	179Y1A0468	ECE	V SEM	
26.	Konda Kondaiah	179Y1A0469	ECE	V SEM	
27.	Konkala Dharani	179Y1A0470	ECE	V SEM	
28.	Kora Lakshmi Prasanna	179Y1A0471	ECE	V SEM	
29.	Kovelakuntla Shaik Abdul Kalam	179Y1A0472	ECE	V SEM	
30.	Lomada Jaya Sree	179Y1A0473	ECE	V SEM	
31.	Majjari Sreekanth	179Y1A0475	ECE	V SEM	
32.	Mallireddy Maheswara Reddy	179Y1A0476	ECE	V SEM	
33.	Mallu Jyothi	179Y1A0477	ECE	V SEM	
34.	MALLU PAVITHRA	179Y1A0478	ECE	V SEM	
35.	Manneti Srikanth Reddy	179Y1A0480	ECE	V SEM	
36.	Mesha Divya Sree	179Y1A0481	ECE	V SEM	
37.	Moyellacheruvu Raghava	179Y1A0483	ECE	V SEM	
38.	Mukkamalla Dadavali	179Y1A0484	ECE	V SEM	
39.	Munagapati Chandana Sai	179Y1A0485	ECE	V SEM	
40.	Muthraipalle Shaik Sajid	179Y1A0486	ECE	V SEM	
41.	Nallabothula Pallavi	179Y1A0488	ECE	V SEM	
42.	Nareddula Ramya	179Y1A0489	ECE	V SEM	
43.	Neelam Pravallika	179Y1A0490	ECE	V SEM	
44.	Obu Swathi	179Y1A0492	ECE	V SEM	
45.	Obulareddy Gari Manoja Reddy	179Y1A0493	ECE	V SEM	
46.	P Nazma	179Y1A0494	ECE	V SEM	

47.	Pagala Prathyusha	179Y1A0496	ECE	V SEM	
48.	Pasavala Venkata Ramana	179Y1A0499	ECE	V SEM	
49.	Pathakuntla Ushasree	179Y1A04A0	ECE	V SEM	
50.	Peddiviti Narasimha	179Y1A04A3	ECE	V SEM	
51.	Pichala Vinod Kumar Reddy	179Y1A04A4	ECE	V SEM	
52.	Pogili Sivalahari	179Y1A04A5	ECE	V SEM	
53.	Polepalli Vijaya Vani	179Y1A04A6	ECE	V SEM	
54.	Ramachandrappa Gari Bharath	179Y1A04A9	ECE	V SEM	
55.	Ranadhir Reddy U	179Y1A04B0	ECE	V SEM	
56.	Rangareddigari Nithya Sree	179Y1A04B1	ECE	V SEM	
57.	Rudraraju Charan Kumar Raju	179Y1A04B3	ECE	V SEM	
58.	Sampathi Reddy Eswarsai	179Y1A04B4	ECE	V SEM	
59.	Shaik Athar	179Y1A04B6	ECE	V SEM	
60.	Shaik Mohammad Shakeer	179Y1A04B9	ECE	V SEM	
61.	Shaik Mohammed Sharif	179Y1A04C0	ECE	V SEM	
62.	Shaik Noor Mohammed	179Y1A04C1	ECE	V SEM	
63.	Shaik Shavalli	179Y1A04C2	ECE	V SEM	
64.	Shaik Tanveer	179Y1A04C3	ECE	V SEM	
65.	Subbraveti Sai Akhil	179Y1A04C4	ECE	V SEM	
66.	Sunkesula Preethi	179Y1A04C5	ECE	V SEM	

Coordinators

HoD

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
KADAPA - 516 003

Syllabus of Certification Course

Course name : MSP 430 launchpad programming

Course objectives:

1. This course will introduce you to the MSP430 and embedded software in general.
2. You will also learn how to implement a basic task scheduler. From setting up ports and registers, to more advanced subjects like callback functions, structs, and timers,
3. you will learn how to program an MSP430 to do precisely timed tasking in a fairly simple manner.

Course outcomes:

After studying this course, students will be able to:

1. Understand the architectural features and instruction set of 16 bit microcontroller MSP430.
2. Develop programs using the various instructions of MSP430 for different applications.
3. Understand the functions of the various peripherals which are interfaced with MSP430 microcontroller.
4. Describe the power saving modes in MSP430.
5. Explain the low power applications using the MSP430 microcontroller.

UNIT-I

MSP430 Architecture:

Introduction –Where does the MSP430 fit, the outside view, The inside view-Functional block diagram, Memory, Central Processing Unit, Memory Mapped Input and Output, Clock Generator, Exceptions: Interrupts and Resets, MSP430 family.

UNIT-II

Addressing Modes & Instruction Set-

Addressing Modes, Instruction set, Constant Generator and Emulated Instructions, Program Examples. Module-3 Clock System, Interrupts and Operating Modes.

UNIT-III

Clock System, Interrupts and Operating Modes-

Clock System, Interrupts, What happens when an interrupted is requested, Interrupt Service Routines, Low Power Modes of Operation, Watchdog Timer, Basic Timer1, Real Time Clock, Timer-A: Timer Block, Capture/Compare Channels, Interrupts from Timer-A.

UNIT-IV

Analog Input-Output and PWM -

Comparator-A, ADC10, ADC12, Sigma-Delta ADC, Internal Operational Amplifiers, DAC, Edge Aligned PWM, Simple PWM, Design of PWM. LCD interfacing.

UNIT-V

Digital Input-Output and Serial Communication:

Parallel Ports, Lighting LEDs, Flashing LEDs, Read Input from a Switch, Toggle the LED state by pressing the push button, LCD interfacing. Asynchronous Serial Communication, Asynchronous Communication with USCI_A, Communications, Peripherals in MSP430, Serial Peripheral Interface.

Textbooks/Reference books:

1.MSP430 LaunchPad Programming Kindle Edition by "Agus Kurniawan"

2.Embedded Systems Design using the MSP430FR2355 LaunchPad by "Brock J. LaMeres"

3.Programmable Microcontrollers with Applications: Msp430 Launchpad with CCS and Grace book review by "Cem unsalan"

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SCHEDULE

Department of ECE

Certification Course

On

"MSP 430 Launchpad programming" From 19/07/2019 to 06/08/2019

Date	Timing	Resource person	Topic to be covered
19-07-2019	3 PM to4PM	Dr.G.Hemalatha	**MSP430 Architecture:** Introduction –Where does the MSP430 fit
19-07-2019	4PM to 5PM	Dr.G.Hemalatha	The outside view
20-07-2019	4PM to 5PM	Smt.K.Divyalakshmi	The inside view
20-07-2019	3PM to 5PM	Smt.K.Divyalakshmi	Functional block diagram,
22-07-2019	4PM to 5PM	Dr.G.Hemalatha	Memory, Central Processing Unit.
22-07-2019	4PM to 5PM	Dr.G.Hemalatha	Memory Mapped Input and Output
23-07-2019	3PM to 5PM	Smt.K.Divyalakshmi	Clock Generator, Exceptions
23-07-2019	4PM to 5PM	Smt.K.Divyalakshmi	Interrupts and Resets, MSP430 family.
24-07-2019	3PM to 5PM	Dr.G.Hemalatha	**Addressing Modes & Instruction Set:** Addressing Modes,
24-07-2019	4PM to 5PM	Dr.G.Hemalatha	Instruction set,
25-07-2019	3PM to 5PM	Smt.K.Divyalakshmi	Constant Generator and Emulated Instructions
25-07-2019	4PM to 5PM	Smt.K.Divyalakshmi	Program Examples.
26-07-2019	3PM to 5PM	Dr.G.Hemalatha	Module-3Clock System,
26-07-2019	4PM to 5PM	Dr.G.Hemalatha	Interrupts and Operating Modes
27-07-2019	3PM to 5PM	Smt.K.Divyalakshmi	**Clock System, Interrupts and Operating Modes:** Clock System, Interrupts
27-07-2019	4PM to 5PM	Smt.K.Divyalakshmi	What happens when an interrupted is requested,
29-07-2019	3PM to 5PM	Dr.G.Hemalatha	Interrupt Service Routines,
29-07-2019	4PM to 5PM	Dr.G.Hemalatha	Low Power Modes of Operation, Watchdog Timer,
30-07-2019	3PM to 5PM	Smt.K.Divyalakshmi	Basic Timer1, Real Time Clock, Timer-A: Timer Block,
30-07-2019	4PM to 5PM	Smt.K.Divyalakshmi	Capture/Compare Channels, Interrupts from Timer-A
31-07-2019	3PM to 5PM	Dr.G.Hemalatha	**Analog Input-Output and PWM :**

			Comparator-A, ADC10, ADC12, Sigma-Delta ADC
31-07-2019	4PM to 5PM	Dr.G.Hemalatha	Internal Operational Amplifiers, DAC, Edge Aligned PWM,
01-08-2019	3PM to 5PM	Smt.K.Divyalakshmi	Simple PWM, Design of PWM. LCD interfacing.
01-08-2019	4PM to 5PM	Smt.K.Divyalakshmi	**Digital Input-Output and Serial Communication:** Parallel Ports, Lighting LEDs,
02-08-2019	3PM to 5PM	Dr.G.Hemalatha	Flashing LEDs, Read Input from a Switch.
02-08-2019	4PM to 5PM	Dr.G.Hemalatha	Toggle the LED state by pressing the push button
03-08-2019	3PM to 5PM	Smt.K.Divyalakshmi	LCD interfacing. Asynchronous Serial Communication,
03-08-2019	4PM to 5PM	Smt.K.Divyalakshmi	Asynchronous Communication with USCI_A,
05-08-2019	4PM to 5PM	Dr.G.Hemalatha	Communications, Peripherals in MSP43 Serial Peripheral Interface.
06-08-2019	4PM to 5PM	Dr.G.Hemalatha Smt.K.Divyalakshmi	Valedictory

Coordinator(s)

HoD

Professor & H.O.D.
Department of E.C.E.
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DEPARTMENT OF ECE

Attendance sheet of Certification Course on "MSP 430 Launch pad programming"
From 19/07/2019 to 06/08/2019

S. No.	Roll No.	Name	19/07/2019	20/07/2019	22/07/2019	23/07/2019	24/07/2019	25/07/2019	26/07/2019	27/07/2019	29/07/2019	30/07/2019	31/07/2019	01/08/2019	02/08/2019	03/08/2019	05/08/2019	06/08/2019
1.	179Y1A0418	Bandi Praneeth	P	P	P	P	A	P	P	A	P	P	P	P	P	P	P	P
2.	179Y1A0419	Banthulla Anil Kumar Raju	P	P	P	P	P	P	P	P	A	A	P	P	P	P	P	P
3.	179Y1A0420	Basireddy Mahesh Kumar Reddy	P	P	P	P	A	A	P	P	P	P	P	P	P	P	P	P
4.	179Y1A0422	Bayyarapu Suresh	P	P	P	P	P	P	P	A	A	P	P	P	P	P	P	P
5.	179Y1A0423	Bheemavarapu Vara Lakshmi (W)	P	P	P	A	P	P	P	P	P	P	P	A	P	P	P	P
6.	179Y1A0426	Bukkey Rakesh Naik	P	P	P	P	P	P	A	P	P	P	A	P	P	P	P	P
7.	179Y1A0427	Chagaleti Surya Narayana Reddy	P	P	P	P	P	P	P	A	P	P	P	A	P	P	P	P
8.	179Y1A0428	Chamarthi Sanjeevaraju	P	P	P	P	P	P	P	P	A	P	P	P	A	P	P	P

9.	179Y1A0429	Chavva Jaswitha	P	P	P	P	P	P	P	A	P	A	P	P	P	P	P	P
10.	179Y1A0431	Chilla Venkateswara Reddy	P	P	P	P	A	P	A	P	P	P	P	P	P	P	P	P
11.	179Y1A0433	Dadiboyina Lohitha	P	P	P	P	P	P	P	P	A	A	P	P	P	P	P	P
12.	179Y1A0435	Dara Sekhar	P	P	P	A	P	P	P	P	A	P	P	P	P	P	P	P
13.	179Y1A0436	Devagudi Venkata Subbaiah	P	P	P	P	A	P	P	P	P	A	P	P	P	P	P	P
14.	179Y1A0452	Goparajulu Renuka Harshitha	P	P	P	P	P	A	P	P	P	P	A	P	P	P	P	P
15.	179Y1A0454	Gorla Sushmitha Reddy	P	P	P	P	P	P	P	A	A	P	P	P	P	P	P	P
16.	179Y1A0455	Guduru Harikrishna	P	P	P	P	P	A	P	P	A	P	P	P	P	P	P	P
17.	179Y1A0456	Gundladurthi Balayalla Reddy	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
18.	179Y1A0458	Julakalva Niranjanareddy	P	P	P	P	P	P	A	P	P	P	A	P	P	P	P	P
19.	179Y1A0459	Kalluru Sunandhana	P	P	P	P	P	P	A	P	P	P	P	P	P	P	P	A
20.	179Y1A0460	Kambam Vasu Kalyan Reddy	P	P	P	P	P	P	A	P	P	P	P	P	P	P	P	A
21.	179Y1A0461	Kambella Samba	A	P	P	P	P	P	A	P	P	P	P	P	P	P	P	P
22.	179Y1A0463	Kanala Pramod Kumar Reddy	A	P	P	P	P	P	P	A	P	P	P	P	P	P	P	P
23.	179Y1A0464	Ketha Madhava Reddy	P	P	P	P	P	P	P	P	P	P	A	A	P	P	P	P
24.	179Y1A0467	Kollapudi Keerthana	P	P	P	P	P	P	P	A	P	P	A	P	P	P	P	P
25.	179Y1A0468	Komme Seshu	P	P	P	P	P	P	P	A	P	P	A	P	P	P	P	P
26.	179Y1A0469	Konda Kondaiah	P	P	P	P	P	P	P	P	P	A	A	P	P	P	P	P
27.	179Y1A0470	Konkala Dharani	A	P	P	P	P	P	A	P	P	P	P	P	P	P	P	P
28.	179Y1A0471	Kora Lakshmi Prasanna	P	A	A	P	P	P	P	P	P	P	P	P	P	P	P	P
29.	179Y1A0472	Kovelakuntla Shaik Abdul Kalam	P	P	P	P	P	P	P	A	A	P	P	P	P	P	P	P
30.	179Y1A0473	Lomada Jaya Sree	P	A	A	P	P	P	P	P	P	P	P	P	P	P	P	P
31.	179Y1A0475	Majjari Sreekanth	P	P	P	P	P	P	A	P	A	P	P	P	P	P	P	P
32.	179Y1A0476	Mallireddy Maheswara	P	P	P	P	P	P	P	P	P	A	P	P	A	P	P	P

		Reddy	P	P	P	P	A	P	P	P	A	P	P	P	P	P	P	P	P
33.	179Y1A0477	Mallu Jyothi	P	A	P	P	P	P	P	P	P	P	P	P	P	P	A	P	P
34.	179Y1A0478	MALLU PAVITHRA	P	P	A	P	P	A	P	P	P	P	P	P	P	P	P	P	P
35.	179Y1A0480	Manneti Srikanth Reddy	P	P	P	P	A	P	P	P	A	P	P	P	P	P	P	P	P
36.	179Y1A0481	Mesha Divya Sree	P	P	P	P	P	A	P	P	P	P	P	P	A	P	P	P	P
37.	179Y1A0483	Moyellacheruvu Raghava	P	P	P	P	A	P	P	P	P	P	P	P	P	A	P	P	P
38.	179Y1A0484	Mukkamalla Dadavali	P	P	P	A	P	A	P	A	P	P	P	P	P	P	P	P	P
39.	179Y1A0485	Munagapati Chandana Sai	P	P	P	P	A	P	P	A	P	P	P	P	P	P	P	P	P
40.	179Y1A0486	Muthraipalle Shaik Sajid	P	P	P	P	P	A	P	P	P	P	P	A	P	P	P	P	P
41.	179Y1A0488	Nallabothula Pallavi	P	P	P	A	P	P	P	P	P	P	P	A	P	P	P	P	P
42.	179Y1A0489	Nareddula Ramya	P	P	P	P	P	A	P	P	P	P	A	P	P	P	P	P	P
43.	179Y1A0490	Neelam Pravallika	P	A	P	P	P	P	A	P	P	P	P	P	P	P	P	P	P
44.	179Y1A0492	Obu Swathi	A	P	P	P	P	P	P	P	A	P	P	P	P	P	P	P	P
45.	179Y1A0493	Obulareddy Gari Manoja Reddy	P	A	P	P	P	P	A	P	P	P	P	P	P	P	P	P	P
46.	179Y1A0494	P Nazma	P	P	P	P	P	A	P	P	P	P	A	P	P	P	P	P	P
47.	179Y1A0496	Pagala Prathyusha	P	P	P	P	P	P	P	A	P	P	P	P	A	P	P	P	P
48.	179Y1A0499	Pasavala Venkata Ramana	P	P	P	P	P	A	P	P	P	P	P	P	P	A	P	P	P
49.	179Y1A04A0	Pathakuntla Ushasree	P	P	P	P	A	P	P	A	P	P	P	P	P	P	P	P	P
50.	179Y1A04A3	Peddiviti Narasimha	A	P	P	P	P	P	A	P	P	P	P	P	P	P	P	P	P
51.	179Y1A04A4	Pichala Vinod Kumar Reddy	P	A	P	P	P	A	P	P	P	P	P	P	P	P	P	P	P
52.	179Y1A04A5	Pogili Sivalahari	P	P	P	P	P	P	A	P	P	P	P	P	A	P	P	P	P
53.	179Y1A04A6	Polepalli Vijaya Vani	P	P	P	P	P	A	P	P	P	P	A	P	P	P	P	P	P
54.	179Y1A04A9	Ramachandrappa Gari Bharath	P	P	P	A	P	P	P	P	P	P	P	P	P	P	P	A	P
55.	179Y1A04B0	Ranadhir Reddy U	P	A	P	P	A	P	P	P	P	P	A	P	P	P	A	P	P

56.	179Y1A04B1	Rangareddigari Nithya Sree	P	A	P	A	P	P	P	A	P	P	A	P	P	A	P	A
57.	179Y1A04B3	Rudraraju Charan Kumar Raju	A	A	P	P	A	A	P	A	P	A	P	A	P	A	P	A
58.	179Y1A04B4	Sampathi Reddy Eswarsai	P	P	A	A	P	A	P	P	A	A	P	P	A	P	A	P
59.	179Y1A04B6	Shaik Athar	A	P	A	P	A	P	A	P	A	P	P	P	A	A	P	P
60.	179Y1A04B9	Shaik Mohammad Shakeer	P	P	P	A	P	A	P	A	P	A	P	A	P	A	P	A
61.	179Y1A04C0	Shaik Mohammed Sharif	P	P	P	P	A	A	P	P	A	A	P	P	A	A	P	P
62.	179Y1A04C1	Shaik Noor Mohammed	P	A	P	A	P	A	P	A	P	A	P	A	P	A	P	A
63.	179Y1A04C2	Shaik Shavalli	A	A	P	P	P	A	A	A	P	P	P	P	A	A	A	P
64.	179Y1A04C3	Shaik Tanveer	A	P	A	A	P	A	P	A	P	A	P	A	P	P	P	P
65.	179Y1A04C4	Subbraveti Sai Akhil	P	P	P	A	P	P	A	A	P	A	P	A	P	A	P	A
66.	179Y1A04C5	Sunkesula Preethi	A	A	A	P	A	P	A	P	P	P	A	A	P	A	P	A

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K.S.R.M. COLLEGE OF ENGINEERING

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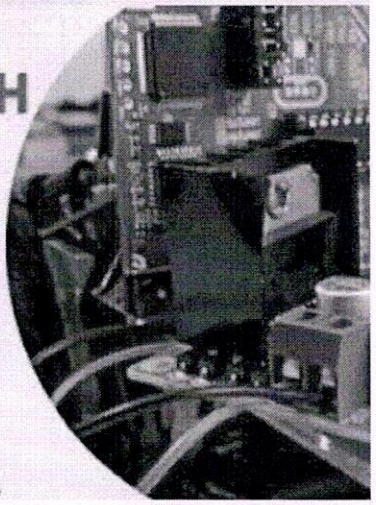
Department of ECE

Certification Course on "MSP430 LAUNCH PAD PROGRAMMING"



Cordinators

19/07/2019 to 06/08/2019

Smt.K.Divya Lakshmi
Asst.Professor, Dept of ECE

Dr.G.Hemalatha
Professor, Dept of ECE

Venue

DSP LAB

Resource Persons

Smt.K.Divya Lakshmi
Asst.Professor, Dept of ECE

Dr.G.Hemalatha
Professor, Dept of ECE

Dr. G. HEMALATHA (Professor & Head)	Dr. V.S.S. Murthy (Principal)	Prof. A. MOHAN (Director)	Sri K. Sivananda Reddy (Correspondent,Secretary,Treasurer)	Sri K. Madan Mohan Reddy (Vice - Chairman)	Sri S. Sankar Reddy (Chairman)

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ACTIVITY REPORT

Certification Course

On

"MSP 430 Launchpad Programming "

From 19th July 2019 to 06th August 2019

Target Group	:	**B.Tech Students**
Details of Participants	:	**66 Students**
Resource persons	:	**Dr.G.Hemalatha Prof, Dept. of ECE**
		Smt .K.Divyalakshmi, Asst.Prof, Dept. of ECE
Coordinators	:	**Dr.G.Hemalatha Prof, Dept. of ECE**
		Smt .K.Divyalakshmi, Asst.Prof, Dept. of ECE
Organizing Department	:	**Department of Electronics and Communication Engineering**
Venue	:	**DSP lab**

Description:

The Certification Course on "MSP 430 Launchpad Programming" was organized by Dept. of ECE from 19/07/2019 to 06/08/2019 . Dr .G.Hemalatha, Smt.K.Divyalakshmi acted as Course instructor. MSP430 Architecture, Addressing Modes & Instruction Set, Clock System, Interrupts and Operating Modes, Analog Input-Output and PWM, Digital Input-Output and Serial Communication were explained.

Photos :

Fig : Resource person delivering the lecture

Fig : Students listening to the lecture.

Coordinators **HoD**

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
KADAPA-516 003

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Kadapa, Andhra Pradesh, India- 516003.

CERTIFICATE OF COMPLETION

This is to certify that Mr./Ms. C. Jaswitha

bearing roll no 17Y91A0429 has Completed a Certification Course on **"MSP430 Launchpad Programming"** organized by the department of **Electronics & Communication Engineering** , KSRM College of Engineering from 19-07-2019 to 06-08-2019.

Coordinator

HoD,ECE

Principal

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Kadapa, Andhra Pradesh, India- 516003.

CERTIFICATE OF COMPLETION

This is to certify that Mr./Ms. D. Sekhar

bearing roll no 179Y1A0435 has Completed a Certification Course on **"MSP430 Launchpad Programming"** organized by the department of **Electronics & Communication Engineering** , KSRM College of Engineering from 19-07-2019 to 06-08-2019.

Coordinator

HoD,ECE

Principal

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CERTIFICATE OF COMPLETION

This is to certify that Mr./Ms. M. Jyothi
bearing roll no 179Y1A0477 has Completed a Certification Course on **"MSP430 Launchpad Programming"** organized by the department of **Electronics & Communication Engineering** , KSRM College of Engineering from 19-07-2019 to 06-08-2019.

Coordinator HoD,ECE Principal

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FEEDBACK FORM

Certification Course on "*MSP 430 Launchpad programming*", from 19-07-2019 to 06-08-2019

Organized

by

Department of Electronics & Communication Engineering

NAME:

Roll No:

S.No	Feedback Item	Excellent	Very Good	Good	Average	Below Average
1	Organization of certificate course and session planning by the instructor.					
2	Clarity in content delivery.					
3	Content is relevant and useful					
4	Adequate opportunity to interact with trainer					
5	Judicious mix of concepts. Principles and practices.					
6	Assignments and tasks are interesting and challenging.					
7	Overall rating					

Any suggestions for improvement.

Signature

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Certification Course on
"MSP 430 Launch pad programming"
19/07/2019 to 06/08/2019

Feedback responses

S.No.	Roll No	Year & Semester	Branch	Is the course content met your expectation	Is the lecture sequence well planned	The contents of the course is explained with examples	Is the level of course high	Is the course exposed you to the new knowledge and practices	Is the lecturer clear and easy to understand	Rate the value of course in increasing your skills	Any issues
1	179Y1A0418	B.Tech Vsem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	3	5	Nothing
2	179Y1A0419	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	3	4	very good
3	179Y1A0420	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Good
4	179Y1A0422	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	4	very good
5	179Y1A0423	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	4	5	Nothing
6	179Y1A0426	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	3	Good
7	179Y1A0427	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	4	Good

8	179Y1A0428	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	4	Nothing
9	179Y1A0429	B.Tech Vsem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Nothing
10	179Y1A0431	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	3	Very Good
11	179Y1A0433	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	5	Good
12	179Y1A0435	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	4	Good
13	179Y1A0436	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	3	5	Nothing
14	179Y1A0452	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	very good
15	179Y1A0454	B.Tech Vsem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	4	Nothing
16	179Y1A0455	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	5	very good
17	179Y1A0456	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	3	No
18	179Y1A0458	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	3	4	Nothing
19	179Y1A0459	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Good
20	179Y1A0460	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	3	3	Good
21	179Y1A0461	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Good
22	179Y1A0463	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	5	Nothing
23	179Y1A0464	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	4	Good
24	179Y1A0467	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	4	4	Good
25	179Y1A0468	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	4	Good

26	179Y1A0469	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	5	Nothing
27	179Y1A0470	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	3	No
28	179Y1A0471	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	4	No
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32	179Y1A0476	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	3	Nothing
33	179Y1A0477	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	4	No
34	179Y1A0478	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	5	Nothing
35	179Y1A0480	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Good
36	179Y1A0481	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	3	5	Nothing
37	179Y1A0483	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	3	4	very good
38	179Y1A0484	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Good
39	179Y1A0485	B.Tech Vsem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	4	very good
40	179Y1A0486	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	4	5	Nothing
41	179Y1A0488	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	3	Good
42	179Y1A0489	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	4	Good
43	179Y1A0490	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	4	Nothing

44	179Y1A0492	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Nothing
45	179Y1A0493	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	3	Very Good
46	179Y1A0494	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	5	Good
47	179Y1A0496	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	4	Good
48	179Y1A0499	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	3	5	Nothing
49	179Y1A04A0	B.Tech Vsem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	very good
50	179Y1A04A3	B.Tech Vsem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	4	Nothing
51	179Y1A04A4	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	5	very good
52	179Y1A04A5	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	3	No
53	179Y1A04A6	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	3	4	Nothing
54	179Y1A04A9	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Good
55	179Y1A04B0	B.Tech Vsem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	3	3	Good
56	179Y1A04B1	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Good
57	179Y1A04B3	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	5	Nothing
58	179Y1A04B4	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	4	Good
59	179Y1A04B6	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	4	4	Good
60	179Y1A04B9	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	4	Good
61	179Y1A04C0	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	5	Nothing

62	179Y1A04C1	B.Tech V sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	3	No
63	179Y1A04C2	B.Tech Vsem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	4	No
64	179Y1A04C3	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	4	3	No
65	179Y1A04C4	B.Tech Vsem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	4	No
66	179Y1A04C5	B.Tech V sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	4	nothing

Coordinator

HoD

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KADAPA - 516 003.

UNIT-III
MSP 430

Memory

Volatile Memory:

- Loses its contents when power is removed. It is usually called *random-access memory* or RAM.
- The vital feature is that data can be read or written with equal ease. Volatile memory is used for data, and small microcontrollers often have very little RAM, sometimes only a few tens of bytes.

Static RAM:

- means that it retains its data even if the clock is stopped (provided that power is maintained, of course).
- A single cell of static RAM needs six transistors.
- RAM therefore takes up a large area of silicon, which makes it expensive.

Dynamic RAM:

- This needs only one transistor per cell but must be refreshed regularly to maintain its contents, so it is not used in small microcontrollers.
- Most memory in a desktop computer is *dynamic* RAM.

Nonvolatile Memory:

- Retains its contents when power is removed and is therefore used for the program and constant data. It is usually called *read-only memory* or ROM

There are many types of nonvolatile memory in use:

- **Masked ROM:**
- The data are encoded into one of the masks used for photolithography and written into the IC during manufacture. This memory really is read-only.

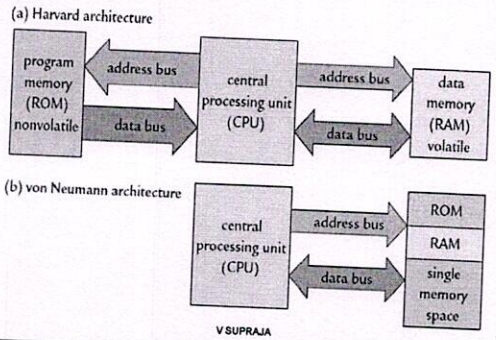
- It is used for the high-volume production of stable products, because any change to the data requires a new mask to be produced at great expense.
- Some MSP430 devices can be ordered with ROM, shown by a *C* in their part number. An example is the MSP430CG4619.
- **EPROM (electrically programmable ROM):**
- As its name implies, it can be programmed electrically but not erased.
- Devices must be exposed to ultraviolet (UV) light for about ten minutes to erase them.
- erasable devices need special packages with quartz windows, which are expensive.

Flash memory:

- This can be both programmed and erased electrically and is now by far the most common type of memory.
- The practical difference is that individual bytes of EEPROM can be erased but flash can be erased only in blocks.
- Most MSP430 devices use flash memory, shown by an *F* in the part number.
- Microcontrollers use **NOR flash**, which is slower to write but permits random access. **NAND flash** is used in bulk storage devices and can be accessed only serially in rows.

Harvard and Von-Neuman Architectures

Block Diagram:



Harvard Architecture:

- The volatile (data) and nonvolatile (program) memories are treated as separate systems.
- Each with its own address and data bus. Many microcontrollers use this architecture, including Microchip PICs, the Intel 8051 and descendents, and the ARM9.
- The principal advantage is efficiency.
- It allows simultaneous access to the program and data memories. For instance, the CPU can read an operand from the data memory at the same time as it reads the next instruction from the program memory.
- Easier to pipeline so high performance can be achieved.
- No memory alignment problems.
- High Cost

von Neumann Architecture:

- Single shared bus for instruction and data fetching.
- There is only a single memory system in the von Neumann or Princeton architecture.
- This means that only one set of addresses covers both the volatile and nonvolatile memories.
- The architecture is intrinsically less efficient because several memory cycles may be needed to extract a full instruction from memory.
- Low performance compared to Harvard architecture.
- It has memory alignment problems.
- Cheaper
- Microcontrollers with a von Neumann architecture include the MSP430, the Freescale HCS08, and the ARM7.

RISC vs CISC

RISC	CISC
Reduced Instruction set Computer	Complex Instruction set Computer
Less number of instructions	More number of instructions
It uses instruction pipelining feature. So, the execution speed is more.	No instruction pipelining feature.
Orthogonal instruction set.	Non Orthogonal instruction set
Operations are performed on registers only, the only memory operations are load and store.	Operations are performed on registers or memory depending on the instruction.
Large number of registers are available	Limited number of general purpose registers
Programmer need to write more code to execute task since instructions are simple ones	Instructions are like macros in C language. Programmer can achieve the desired functionality with single instructions.

Single and fixed length instructions.	Variable length instructions
Less silicon usage and pin count	More silicon usage
It uses harvard or von- neumann architecture.	It uses harvard or von- neumann architecture.
Eg: Atmel AVR contains 32 instructions	Eg: Atmel AT89C51 contains 255 instructions.

INTRODUCTION TO MSP430 MICROCONTROLLERS

- The MSP430 was introduced in the late 1990s
- 16bit processor with a vonNeumann architecture, designed for low-power applications
- The CPU is often described as a reduced instruction set computer (RISC)
- The registers in the CPU are also all 16 bits wide and can be used interchangeably for either data or addresses
- The MSP430 has 16registers in its CPU, which enhanc es efficiency because they can be used for local variables, parameters passed to subroutines, and eith er addresses or data

- Several features make the MSP430 suitable for low-power and portable applications:
- The CPU is small and efficient, with a large number of registers
- It is extremely easy to put the device into a low-power mode. No special instruction is needed
- The crystal runs continuously at 32KHz and is used to wake the device periodically.
- MSP430 can wake from a stand by mode rapidly, perform its tasks, and return to a low-power mode
- A wide range of peripherals is available, many of wh ich can run autonomously without the CPU for most of the time

- Many portable devices include liquid crystal displays which the MSP430 can drive directly.

MSP430 Family:

- The letter after MSP430 shows the type of memory. F – Flash memory, C for ROM
- The second letter shows ASIP. E for Electricity, W for water, G for signals that require a gain stage.
- The next digit shows the family and the final two or three digits identify the specific device

MSP430x1xx:

- Provides a wide range of general purpose devices from simple versions to complete systems for processing signals

- There is a broad selection of peripherals and some include a hardware multiplier, which can be used as rudimentary digital signal processor
- Packages have 20–64 pins

MSP430F2xx:

- Introduced in 2005.
- CPU can run at16 MHz, double the speed of earlier devices, while consuming only half the current at the same speed.
- 14 pin PDIP package .
- Pull-up or pull down resistors are provided on the inputs to reduce the number of external components needed

- Even the smallest,14-pin devices offer a 16-bit sigma–delta ADC.

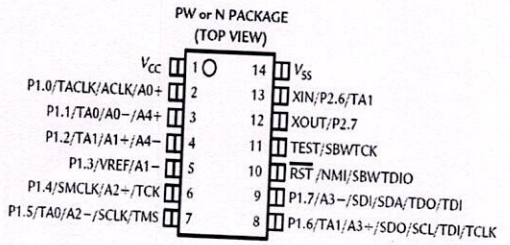
MSP430x3xx:

The original family, which includes drivers for LCDs. It i s now obsolescent.

MSP430x4xx:

- Can drive LCDs with up to 160 segments. Many of th em are ASSPs, but there are general-purpose devices as well. Their packages have 48–113 pins, many of which are needed for the LCD.

MSP430F2003 and F2013 Pin Diagram



MSP430F2003 and F2013 Pin Diagram

- *VCC* and *VSS* , P1.0–P1.7, P2.6, and P2.7 , TACLK, TA0, and TA1 are associated with Timer_A;
- A0–, A0+, and so on, up to A4±, are inputs to the anal og-to-digital converter.
- ACLK and SMCLK are outputs for the microcontroller's clock signals
- SCLK, SDO, and SCL are used for the universal serial int erface
- XIN and XOUT , RST, NMI

TCK, TMS, TCLK, TDI, TDO, and TEST form the full JTAG in terface, used to program and debug the device

- SBWTDIO and SBWTCK provide the Spy-Bi-Wire interface, an alternative to the usual JTAG connection that saves pins

Key Features of MSP430

- a low power Microcontroller released by Texas Instruments in the late 1990s.
- a 16-bit RISC based mixed signal processor.
- with a set of intelligent peripherals like I/O, Timers ADC, DAC, flexible clock and USCI
- low cost
- lowest power consumption
- Ultra low power optimization extends battery life
- multiple low power modes of operation

Contd..

- Extensive interrupt capability relieves need for polling
- Prioritized nested interrupts
- Seven source-address modes
- Four destination-address modes
- Only 27 core instructions and 24 Emulated Instructions
- Large register file
- Efficient table processing
- Fast hex-to-decimal conversion

contd..

- MSP430 requires
  0.1 µA for RAM data Retention,
  0.8 µA for RTC mode operation
  250 µA/MIPS for active mode operation.
- Low operation voltage (from 1.8 V to 3.6 V).
- Zero-power Brown-Out -Reset (BOR)

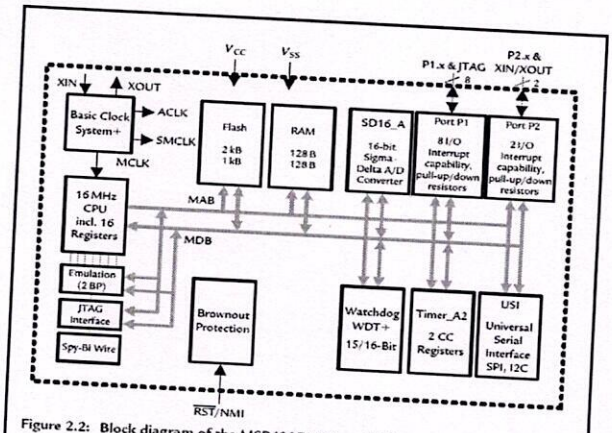


Figure 2.2: Block diagram of the MSP430F2003 and F2013, taken from the data sheet.

MEMORY

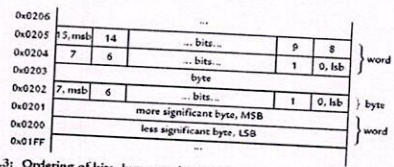


Figure 2.3: Ordering of bits, bytes, and words in memory, adapted from the *MSP430x2xx Family User's Guide*. Addresses increase up the page.

- The MSP430X extends the range of memory by a factor of 16 to 20 bytes by adding a further 4 bits to the address bus and the registers in the CPU.
- Byte accessing and Word accessing.
- Two bytes at 0x0200 and 0x0201 can be considered as a valid word with address 0x0200

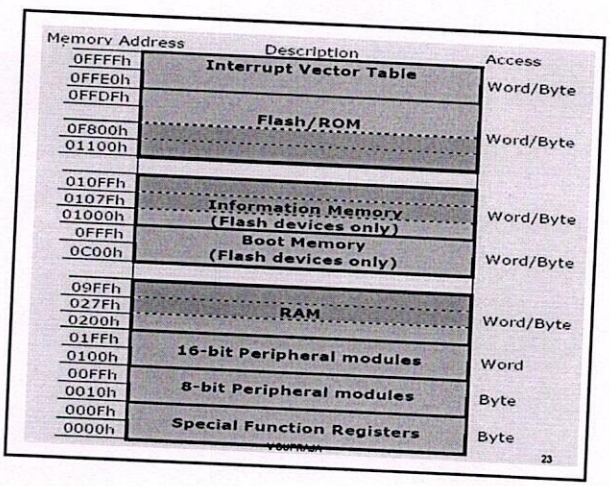
- Hexadecimal value 0x1234

Little-endian ordering: The low-order byte is stored at the lower address and the Higherorder byte at the higher address. This is used byte MSP430 and is the more common format.

Big-endian ordering: The high-order byte is stored at the lower address. This is use dby the Freescale HCS08.

- Addresses increase from left to right across each line. This means that the low-order byte is displayed first, followed by the high-order byte. Thus our value of

0x1234 is displayed as 34 12.



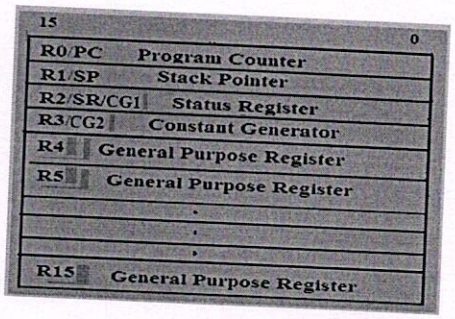
MSP430 CPU

- The CPU of MSP 430 includes a 16-bit ALU and a set of 16 Registers R0 –R15.In these registers Four are special Purpose and 12 are general purpose registers . All the registers can be addressed in the same way.

The special Purpose Registers are

- PC (Program Counter), SP (Stack Pointer) , SR (Status Register) and CGx (Constant Generator)

Registers in the CPU of the MSP430



- The MSP430 CPU includes an arithmetic logic unit (ALU) that handles addition, subtraction, comparison and logical (AND, XOR) operations. ALU operations can affect the overflow, zero, negative, and carry flags in the status register.

R0: Program Counter (PC)

- The 16-bit Program Counter (PC/R0) points to the next instruction to be read from memory and executed by the CPU. The Program counter is incremented by 2. It is important to note that the PC is aligned at even addresses, because the instructions are 16 bits, even though the individual memory addresses contain 8-bit values.
- Subroutines and interrupts also modify the PC but in these cases the previous value is saved on the stack and restored later

R1: Stack Pointer (SP)

- The Stack Pointer (SP/R1) is located in R1.
- Stack can be used by user to store data for later use(instructions: store by PUSH, retrieve by POP)
- Stack is also heavily used for temporary variables, passing parameters to subroutines and returning the result.
- The stack is allocated at top of RAM and grows down towards the low address. SP holds the address of top of the stack.

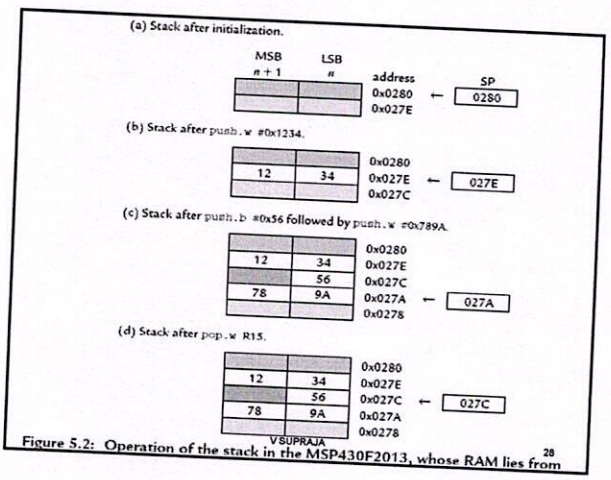


Figure 5.2: Operation of the stack in the MSP430F2013, whose RAM lies from

Contd..

- For programs written in C, the compiler initializes the stack automatically as part of the startup code, which runs silently before the program starts, but *you must initialize SP yourself in assembly language.*

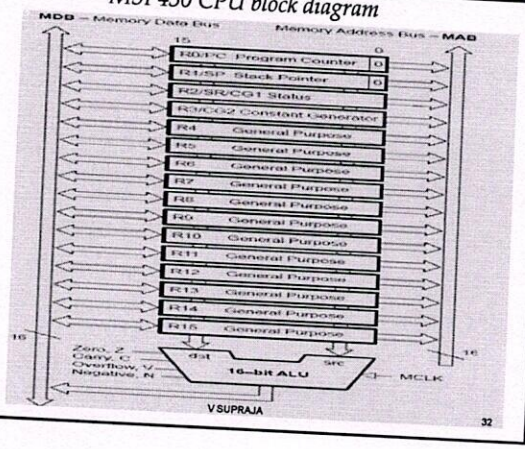
R2: Status Register (SR)

The Status Register (SR/R2) is a 16 bit register , and it stores the state and control bits. The system flags are changed automatically by the CPU depending on the result of an operation in a register. The reserved bits of the SR are used to support the constants generator.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved for CG1							V	SCG1	SCG0	OSCOFF	CPUOFF	GIE	N	Z	C

- The hexadecimal sum 0x75+0xC7=0x13C, where the result is too large to be held in a single byte
- The *zero flag Z is set when the result of an operation is 0.*
- The *negative flag N is made equal to the msb of the result, which indicates a* negative number if the values are signed.
- The *signed over low flag V is set when the result of a signed operation has* overflowed, even though a carry may not be generated
- Remember that a byte can hold the values 0 to 0xFF if it is unsigned or −0x80 to 0x7F if it is signed.

MSP430 CPU block diagram



Enable Interrupts

- Setting the *general interrupt enable or GIE bit enables maskable interrupts, provided that* the individual sources of interrupts have themselves been enabled.
- Clearing the bit disables all maskable interrupts.

Control of Low-Power Modes

- The CPUOFF, OSCOFF, SCG0, and SCG1 bits control the mode of operation of the MCU. All systems are fully operational when all bits are clear. Setting combinations of these bits puts the device into one of its low-power modes.

R2/R3: Constant Generator Registers (CG1/CG2)

- Depending on the source-register addressing modes (As) value, six commonly used constants can be generated without a code word or code memory access to retrieve them. This is a very powerful feature, which allows the implementation of emulated instructions, for example, instead of implementing a core instruction for an increment, the constant generator is used.

R4 - R15: General–Purpose Registers

- These general-purpose registers are used to store data values , address pointers, or index values and can be accessed with byte or word instructions.

Addressing modes

The MSP430 supports seven addressing modes for the source operand and four addressing modes for the destination operand . They are

- Register mode
- Indexed mode
- Symbolic mode
- Absolute mode
- Indirect register mode
- Indirect auto incrément mode
- Immediate mode

Register Mode

- Register mode operations work directly on the processor registers, R4 through R15, or on special function registers, such as the program counter or status register. They are very efficient in terms of both instruction speed and code space.

Ex : MOV.b R4, R5

MOV.W R4,R5

Move (copy) the contents of source (register R4) to destination (register R5). Register R4 is not affected.

Indexed mode

- The Indexed mode commands are formatted as X(Rn), where X is a constant and Rn is one of the CPU registers. The absolute memory location X+Rn is addressed.
- Indexed mode addressing is useful for applications such as lookup tables

Ex : MOV. b F000h(R5), R4

Move (copy) the contents at source address (F000h +R5) to destination (register R4)

Symbolic mode

- Symbolic mode allows the assignment of labels to fixed memory locations, so that those locations can be addressed. This is useful for the development of embedded programs.
- MOV XPT, YPT; Move the content of source address XP (x pointer) to the destination address YPT (y pointer).
- MOV.w LoopCtr, R6; Load word loopCtr into R6
- Assemler replaces this by the indexed form
- Mov.w X(PC), R6; Load word loopCtr into R6
- Where X= LoopCtr-PC

Absolute mode

- Similar to Symbolic mode, with the difference that the label is preceded by "&".

The word following the instruction contains the absolute address. X is stored in the next word. Indexed mode X(SR) is used

MOV &XPT, &YPT; Move the content of source address XPT to the destination address YPT.

Eg1: mov.b &P1IN, R6; Load byte P1IN into R6.

Assemler replaces this by the indexed form

Mov.b P1IN(SR), R6; Load byte P1IN into R6.

Assemler replaces this by the indexed form.

P1IN is the absolute address of the register.

SP- Relative Mode

- The stack pointer SP can be used as the register in indexed mode like any other
- Suppose that we wanted to copy the value that had been pushed onto the stack before the most recent one

Eg: mov.w 2(SP),R6 *; copy most recent word but one fr*

- For example, suppose that the stack were as shown in Figure 5.2(d) with SP=0x027C. Then the preceding instruction would load 0x1234 into R6.

Indirect register mode

- The data word addressed is located in the memory location pointed to by Rn. Indirect mode is not valid for destination operands, but can be emulated with the indexed mode format @(Rn). Here Rn is used as a pointer to the operand.
- MOV @(R4), R5
- Move the contents of the source address (contents of R4) to the destination (register R5). Register R4 is not modified

Indirect Register Mode

- This is available only for the source and is shown by the symbol @ in front of a register, such as @R5. It means that the contents of R5 are used as the *address of the operand.*
- *Eg:* **mov.w @R5 ,R6 *; load word from address (R5)=4 into R6***

Indirect auto increment mode

- Similar to indirect register mode, but with indirect auto increment mode, the operand is incremented as part of the instruction. The format for operands is @Rn+. This is useful for working on blocks of data.
- Rn is used as a pointer to the operand. Rn is incremented afterwards by 1 for byte instructions and by 2 for word instructions.

Ex: MOV @R4+, R5

Move the contents of the source address (contents of R4) to the destination (register R5), then increment the value in register R4 to point to the next word.

Immediate mode

- Immediate mode is used to assign constant values to registers or memory locations.
- MOV #E2h, R5
- Move the immediate constant E2h to the destination (register R5).

Instruction set

- The MSP430 instruction set consists of 27 core instructions. Additionally, it supports 24 emulated instructions. The core instructions have unique op-codes decoded by the CPU, while the emulated ones need assemblers and compilers to generate their mnemonics.
- There are three core-instruction formats:
- Double operand (Format I)
- Single operand (Format II)
- Program flow control – Jump (Format III)

Contd..

- The instruction set is orthogonal *with* few exceptions, meaning that all addressing modes can be used with all instructions and registers.
- The emulated instructions use core instructions combined with the architecture and implementation of the CPU for higher code efficiency and faster execution.

Movement Instructions

- There is only the one 'mov' instruction to move data. It can address all of memory as either source or destination, including both registers in the CPU and the whole memory map.

- **Ex : mov . w src , dst**

Here . w denotes that the operations can use either bytes or words

Stack Operations

- These instructions either push data onto the stack or pop them off .

ex 1: push .w src ; push data onto stack

ex 2 : pop .w dst ; pop data off stack.

The pop operation is emulated using post-increment addressing but push requires a special instruction because pre-decrement addressing is not available.

Arithmetic and Logic Instructions with Two Operands

- add.w src ,dst ; add
- addc.w src ,dst ; *add with carry*
- adc.w dst ; *add carry bit*
- sub.w src ,dst ; *subtract*
- subc.w src ,dst ; *subtract with borrow*
- sbc.w dst ; *subtract borrow bit*
- cmp.w src ,dst ; *compare , set flags only.*

The compare operation cmp is the same as subtraction except that only the bits in SR are affected ; the result is not written back to the destination.

Arithmetic Instructions with One Operand

- All these are instructions are emulated, which means that the operand is always a destination.
- Ex: clr.w dst ; *clear*
- dec.w dst ; *decrement*
- decd.w dst ; *double decrement*
- inc.w dst ; *increment*
- incd.w dst ; *double increment*
- tst.w dst ; *test (compare with 0)*

Decimal Arithmetic

- These instructions are used when operands are binary-coded decimal (BCD) rather than ordinary binary values.
- Ex : dadd.w src , dst ; decimal add with carry.
- dadc.w dst ; decimal add carry bit

Logic Instructions with Two Operands

- The MSP430 has the usual and and exclusive-OR xor instructions. The and and bitwise test operations are identical except that bit is only a test and does not change its destination.
- Ex : and.w src ,dst ; *bitwise and .*
- xor.w src ,dst ; *bitwise exclusive or*
- bit.w src ,dst ; *bitwise test , set flags only*
- bis.w src ,dst ; *bit set; Not.src.and.dst*
- bic.w src ,dst ; *bit clear;src.or.dst*

Logic Instructions with One Operand

- There is only one instruction of this type . invert 'inv' instruction , also known as ones complement ,which changes all 0 bits to 1 and 1s to 0.
- Ex : inv.w dst ; invert bits

Byte Manipulation

- These instructions do not need a suffix because the size of. the operands is fixed.
- Ex : Swpb src ; swap upper and lower bytes (word only)
- Ex : sxt src *; extend sign of lower byte (word only)*
- The swap bytes instruction 'swpb' swaps the two bytes in a word.
- The sign extend instruction sxt is used to convert a signed byte into a signed word.

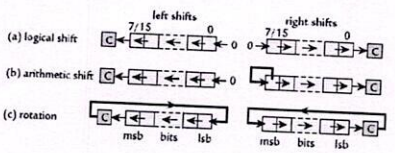
Operations on Bits in Status Register

- There is a set of emulated instructions to set or clear the four lowest bits in the status register and these can be masked using the constant generator.
- Ex: clrc ; clear carry bit.
- clrn ; clear negative bit.
- clrz ; clear zero bit.
- setc ; set carry bit.
- setn ; set negative bit.
- **setz ; set zero bit.**
- **dint ; disable general interrupts.**
- **eint ; enable general interrupts.**

Shift and Rotate Instructions

There are three types of shifts

(i) logical shift (ii) arithmetic shift (iii) rotation. They are explained below.



Contd..

- Logical shift inserts zeroes for both right and left shifts.
- Arithmetic shift inserts zeroes for left shifts but the most significant bit, which carries the sign, is replicated for right shifts.
- Rotation does not introduce or lose any bits; bits that are moved out of one end of the register are passed around to the other.
- Ex : rla dst *; arithmetic shift left*
- rra src *; arithmetic shift right.*
- rlc dst ; rotate left through carry.
- rrc src *; rotate right through carry*

Flow of Control

- The most common elementary use of call is for a subroutine that begins at a particular label.
- Ex: br src *; branch (go to).*
- call src *; call subroutine.*
- ret *; return from subroutine.*
- reti *; return from interrupt.*
- nop *; no operation (consumes single cycle)*

Jumps(Unconditional and Conditional)

- jmp fits in a single word, including the offset, but its range is limited to about ±1KB from the current location.
- jmp label *; unconditional jump.*

Contd..

- The conditional jumps are the "decision-making" instructions and test certain bits or combinations in the status register.
- Ex : jc label *; jump if carry set*
- jnc label *; jump if carry not set ,*
- jn label *; jump if negative ,*
- jz label *; jump if zero*
- jnz label *; jump if nonzero.*
- jge label *; jump if greater or equal ,*
- jl(t) label *; jump if less than*

Instruction Timing

- It takes one cycle to fetch the instruction word itself. This is all if both source and destination are in CPU registers.
- One more cycle is needed to fetch the source if it is given indirectly as @Rn or @Rn+, in which case the address is already in the CPU.
- Alternatively, two more cycles are needed if one of the indexed modes is used. The first is to fetch the base address, second cycle is necessary to fetch the operand itself. This includes absolute and symbolic modes

Table 5.1: Number of MCLK cycles required for typical instructions. It applies only to logical and arithmetic instructions and when the destination is not PC.

Format I destination	Source Rs	Source @Rs, @Rs+	Source S(Rs)
Rd	1	2	3
D(Rd)	4	5	6
Format II	1	3	4

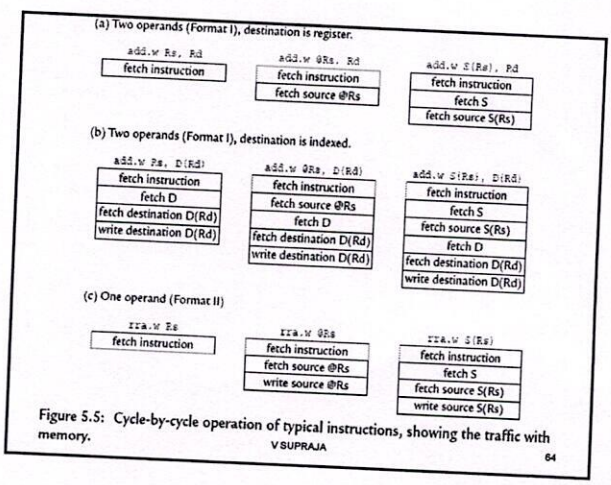


Figure 5.5: Cycle-by-cycle operation of typical instructions, showing the traffic with memory.

Machine Code

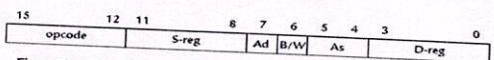


Figure 5.6: Breakdown of a Format I (double operand) instruction.

opcode **(4 bits) is the operation code.**

S-Reg and D-Reg **(4 bits each) specify the CPU registers associated with the** source and destination; the registers either contain the operands themselves or their contents are used to form the addresses

As (2 bits) gives the mode of addressing for the source, which has four basic modes

As Bits		Addressing Mode
0	0	Register
0	1	Indexed
1	0	Indirect Reg.
1	1	Immediate

- **Ad (1 bit) similarly gives mode of addressing for the destination, which has only** two basic modes.

As Bit	Addressing Mode
0	Register
1	Indexed

- **B/W (1 bit) chooses whether the operand is a byte (1) or a word (0).**
- **mov.w R5 ,R6 *; 4506***
- The instruction can be broken into its fields of opcode = 4, S-reg = 5, Ad = 0, B/W = 0, As = 0, D-reg = 6

- The opcode of 4 represents a move.
- The bit B/W = 0 shows that the operand is a word.
- The addressing mode for the source is As = 0, which is register. The register is S-reg = 5, which is R5 as expected.
- Similarly, the addressing mode for the destination is Ad = 0, which again means register. The register is D-reg = 6 = R6.

Eg2: **add.w R5 ,R6 *; 5506***

Eg3: **mov.w #5,R6 *; 4036 0005***

- Now there are two words. The fields of the instruction are opcode = 4, S-reg = 0, Ad = 0, B/W = 0, As = 3 = 11b, D-reg = 6. The difference is in the specification of the source, which means auto increment. The register is Sreg = 0, which is the PC

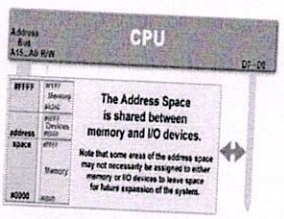
Eg3: mov.b #4,R6 *; 4266*

- This breaks into opcode = 4, S-reg = 2, Ad = 0, B/W = 1, As = 2 = 10b, D-reg = 6. The B/W bit flags a byte rather than a word. The source appears to have indirect register mode on R2/SR/CG1, but this is translated by the constant generator into a value of 0x0004, as required.

ILLEGAL INSTRUCTIONS

- a reset is generated if the CPU tries to fetch an instruction from the range of memory allocated to the special function and peripheral registers (addresses below 0x0200)
- Data can be fetched from a nonexistent address: empty regions of the memory map. Execution proceeds as normal but the "fetched" value is random.
- Data for a word should be aligned to even addresses but you could attempt to fetch a word from an odd address
- Accessing peripheral registers with word access. It is possible to read the lower byte alone but not the upper Byte. An attempt to read the upper byte returns the lower byte instead.

Memory Mapped Input and Output



➢The MSP430 uses *memory-mapped input* and output. This means that the ports simply appear to the CPU as particular memory registers called *peripheral registers*
➢These registers can be read, written and modified in almost the same way as simple registers in RAM. You can even do arithmetic with them, with some restrictions

- **Port P1 input, P1IN:** Reading returns the logical values on the inputs if they are configured for digital input and output. This register is read-only. It is also *volatile*, which means that it may change at a time that a program cannot predict.
- **Port P1 output, P1OUT:**Writing sends the value to be driven onto the pin if it is configured as a digital output. If the pin is not currently an output, the value is stored in a buffer and appears on the pin if it is later switched to be an output.
- **Port P1 direction, P1DIR: A bit of 0 configures the pin as an input, which is the** default. Writing a 1 switches the pin to become an output.

MSP430F5529IPNFunctional Block Diagram

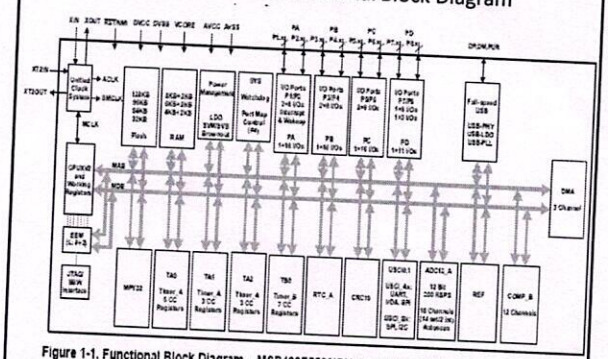
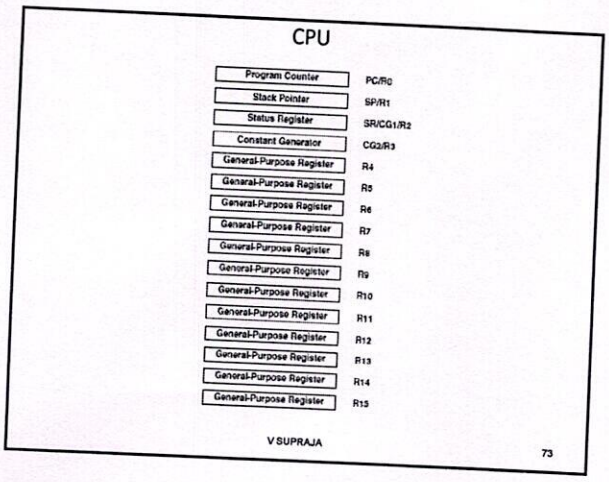


Figure 1-1. Functional Block Diagram – MSP430F5529IPN, MSP430F5527IPN, MSP430F5525IPN, MSP430F5521IPN


CPU
Program Counter
PC/R0
Stack Pointer
SP/R1
Status Register
SR/CG1/R2
Constant Generator
CG2/R3
General-Purpose Register
R4
General-Purpose Register
R5
General-Purpose Register
R6
General-Purpose Register
R7
General-Purpose Register
R8
General-Purpose Register
R9
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