BOARD OF STUDIES MEETING – 2021-22

K.S.R.M COLLEGE OF ENGINEERING

AUTONOMOUS

Minutes of the Meeting

Date	**29.09.2021**	**Day**	**Tuesday**
Time	**10.30 AM**	**Venue**	**Virtual meeting: https://meet.google.com/zub-dxuo-cuv**
Dept.	**ECE**	**Convener**	**Dr. G. Hemalatha**

Members Present:10

S.No	Name	Designation	Signature
1.	Prof. G. Hemalatha	Prof., & HOD ECE, KSRMCE	G. H
2.	Prof. K. Rama Naidu	University nominee Professor in ECE, JNTUA Ananthapuramu	
3.	Prof. M. Rama Subba Reddy	Subject Expert Professor in ECE IIT Madras	
4.	Dr. V. Anil Kumar	Subject Expert Asso.Prof.in ECE IIIT, Hyderabad	M.V.N
5.	Dr. M. Venkatanarayana	Prof., KSRMCE	

Members Absent: 02

S.No	Name	Designation
1	Sri M. Nagendra Kumar	Alumni Member Research Staff CRL, BEL
2	Sri B. Prabhakar	Industry S. V. P. Networks Bangalore

6.	Sri R.V. Sreehari	Asso. Prof., in ECE KSRMCE	
7.	Dr. S. L. Prathapa Reddy	Asso. Prof., in ECE KSRMCE	
8.	Dr. S. Zahiruddin	Asso. Prof., in ECE KSRMCE	
9.	Sri A. Valli Bhasha	Asso. Prof., in ECE KSRMCE	
10.	Sri Md. Mahaboob Pasha	Asso. Prof., in ECE KSRMCE	

Dr. G. Hemalatha, welcomed all the members to the meeting and presented the agenda of the meeting. The resolution sare:

	To do item	Discussion	Resolution	Coordinator/in-charge
1	Approve R-20 UG structure	The Head of the Department has presented the R-20 UG structure designed, Including New Courses recommended Based on the Feedback given by the Stack holders and Action taken Reports and comparing with premier institute syllabus.	The committee approved the R-20 UG structure with a suggestion to introduce Machine learning in the VI semester.	Dr. G. Hemalatha

2	Approve the Syllabus for R-20 UG program III&IV semesters.	The Head of the Department has presented the III&IV semester's syllabus designed, Including New Courses recommended Based on the Feedback given by the Stack holders and Action taken Reports and comparing with premier institute syllabus	The committee has approved curriculum and syllabus for R-20 UG program III&IV semesters with little modifications. To rename the IV unit in Signals and Systems as "Response of LTI Systems". To introduce network synthesis in "Network Theory". To include Differential amplifier in "Linear and Digital IC Applications". To include MOSFET experiments in "Analog Circuits Lab".	M. Mahaboob Pasha
3	To approve structure and syllabi of M. Tech. Embedded Systems and VLSI program.	The HOD has structure and syllabi of M. Tech. Embedded Systems and VLSI program.	The committee approved the structure and syllabi of M. Tech. Embedded Systems and VLSI program.	Dr. M. V. Narayana

The Head of the Department have proposed the Vote of thanks and concluded the meeting.

Convener

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ECE BoS

KSRM College of Engineering (Autonomous) Kadapa

R 20 I & II Semesters Curriculum and syllabus

DEPARTMENT OF ECE

I Semester

S.No	Course code	Category	Course Name	L	T	P	IM	EM	CR
1.	2021101	BSC	Linear Algebra and Calculus	3	0	0	40	60	3
2.	20AP102	BSC	Applied Physics	3	0	0	40	60	3
3.	2024103	HS	Communicative English	3	0	0	40	60	3
4.	2002104	ESC	Fundamentals of Electrical Engineering	3	0	0	40	60	3
5.	2003105	ESC	Engineering Drawing	1	0	2	40	60	2
6.	2003106	ESC	Engineering Drawing Lab	0	0	2	40	60	1
7.	20AP107	BSC	Applied Physics Lab	0	0	3	40	60	1.5
8.	2024108	HS	Communicative English Lab	0	0	3	40	60	1.5
9.	2002109	ESC	Fundamentals of Electrical Engineering Lab	0	0	3	40	60	1.5
									19.5

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II Semester

S. No	Course code	Category	Course Name	L	T	P	IM	EM	CR
1.	2021201	BSC	Differential Equations and Vector Calculus	3	0	0	40	60	3
2.	2023202	BSC	Chemistry	3	0	0	40	60	3
3.	2005203	ESC	C-Programming & Data Structures	3	0	0	40	60	3
4.	2004204	ESC	Electronic Devices & Circuits	3	0	0	40	60	3
5.	20EW205	LC	Engineering Workshop	0	0	3	40	60	1.5
6.	2005206	LC	IT Workshop	0	0	3	40	60	1.5
7.	2023207	BSC	Chemistry Lab	0	0	3	40	60	1.5
8.	2005208	ESC	C-Programming & Data Structures Lab	0	0	3	40	60	1.5
9.	2004209	ESC	Electronic Devices & Circuits Lab	0	0	3	40	60	1.5
10.	20MC210	MC	Environmental Science	3	0	0	30	0	0.0
									19.5

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COURSE STRUCTURE – R20 REGULATIONS
Department of ECE
Proposed Course Structure (R20) – II Year

Semester-III									
S.No	**Code**	**Course Name**	**Category**	**L**	T	**P**	**IM**	**EM**	**Credits**
1.	2021301	Special Functions and Complex Analysis	BSC	3	0	0	40	60	3
2.	2004301	Signals and Systems	PC	3	0	0	40	60	3
3.	2004302	Digital System Design	PC	3	0	0	40	60	3
4.	2004303	Analog Circuits	PC	3	0	0	40	60	3
5.	2004304	Network Theory	PC	3	0	0	40	60	3
6.	2004305	Simulation Lab	PC	0	0	3	40	60	1.5
7.	2004306	Digital System Design Lab	PC	0	0	3	40	60	1.5
8.	2004307	Analog Circuits Lab	PC	0	0	3	40	60	1.5
9.	20SC308	Python Programming (Skilled Course - I)	SC	1	0	2	40	60	2
10.	20MC309	Universal Human Values	MC	3	0	0	40		0
						Total			**21.5**

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Semester-IV									
S.No	**Code**	**Course Name**	**Category**	**L**	T	**P**	**IM**	**EM**	**Credits**
1.	2025401	Business Economics and Accounting for	BSC	3	0	0	40	60	3
2.	2021403	Probability Theory & Stochastic Processes	HSC	3	0	0	40	60	3
3.	2004403	Microprocessors and Microcontrollers	PC	3	0	0	40	60	3
4.	2004404	Electro Magnetic Waves and Transmission Lines	PC	3	0	0	40	60	3
5.	2004405	Linear and Digital IC Applications	PC	3	0	0	40	60	3
6.	2004406	Linear and Digital IC Applications Lab	PC	0	0	3	40	60	1.5
7.	2004407	Microprocessors and Microcontrollers Lab	PC	0	0	3	40	60	1.5
8.	2004408	LabView Programming Lab	PC	0	0	3	40	60	1.5
9.	20SC409	PCB Design (Skilled Course –II)	SC	1	0	2	40	60	2
						Total			**21.5**
		Community Service Project(Mandatory) for 6 weeks duration during summer vacation							

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M.Tech Embedded Systems and VLSI Course Structure

Semester-I									
S.No	Course Code	Course Name	Category	L	T	P	IM	EM	Credits
1.	1854101	RTL Simulation and Synthesis with PLDs	PC	3	0	0	40	60	3
2.	1854102	Microcontrollers and Programmable Digital Signal Processors	PC	3	0	0	40	60	3
3.	1854103	Research methodology and IPR	PC	2	0	0	40	60	2
4.	1854104 1854105 1854106 1854107	1. Parallel Processing 2. Digital Signal and Image Processing 3. VLSI signal processing 4. Design for testability	PE	3	0	0	40	60	3
5.	1854108 1854109 1854110 1854111	1. Programming Languages for Embedded Systems. 2. Micro-Electro Mechanical systems. 3. CAD of Digital System 4. CPLD, FPGA architectures and applications.	PE	3	0	0	40	60	3
6.	1854112	RTL Simulation and Synthesis with PLDs Lab	PC	0	0	4	50	50	2
7.	1854113	Microcontrollers and Programmable Digital Signal Processors Lab	PC	0	0	4	50	50	2
8.	1870A02	Disaster Management	AC				40		0
									18

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Semester-II									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	1854201	Analog and Digital CMOS VLSI Design	PC	3	0	0	40	60	3
2.	1854202	Real Time Operating Systems	PC	3	0	0	40	60	3
3.	1854203 1854204 1854205 1854206	1. Memory Architectures 2. Advanced Computer Architecture 3. SoC Design 4. Low power VLSI Design	PE	3	0	0	40	60	3
4.	1854207 1854208 1854209 1854210	1. Communication Buses and Interfaces 2. Network Security and Cryptography 3. Physical design automation 4. Nanoelectronics	PE	3	0	0	40	60	3
5.	1854211	Analog and Digital CMOS VLSI Design Lab	PC	0	0	4	50	50	2
6.	1854212	Real Time Operating Systems Lab	PC	0	0	4	50	50	2
7.	1854213	Mini Project	PC	0	0	4	100	0	2
8.	1870A01	English for Research paper writing	AC				40		0
									18

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Semester-III									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	1854301 1854302 1854303 1854304	1. IOT and its Applications 2. Hardware Software co-design 3.Artificial Intelligence 4. RFIC Design	PE	3	0	0	40	60	3
2.	1871305 1871306 1871307 1871308 1871309 1871310	1. 5usiness Analytics 2. Industrial Safety 3. Operations Research 4. Cost Management of EngineeringProjects 5. Composite Materials 6. Waste to Energy	OE	3	0	0	40	60	3
3.	1854311	Dissertation Phase -I	Major Project	0	0	20	100	0	10
									16

Semester-IV									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	1854401	Dissertation Phase II	Major Project	0	0	32	50	50	Dissertation Phase II
									16

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Course Title	SIGNALS AND SYSTEMS				B. Tech. ECE III Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
2004301	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

To introduce terminology of signals and systems.

To present Fourier tools through the analogy between vectors and signals.

To teach concept of sampling and reconstruction of signals.

To present linear systems in time and frequency domains.

To teach Laplace and z-transform as mathematical tool to analyze continuous and discrete- time signals and systems.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Identify the various signals and operations on signals.
CO 2	Describe the spectral characteristics of signals.
CO 3	Illustrate signal sampling and its reconstruction.
CO 4	Apply convolution and correlation in signal processing.
CO 5	Analyze continuous and discrete time systems.

UNIT-I

Introduction: Definition and Classification of Signals, Elementary signals, Basic operations on signals.

Fourier series representation of periodic signals: Analogy between vectors and signals, orthogonal signal space, Signal approximation using orthogonal functions, Mean square error, closed or complete set of orthogonal functions, Orthogonality in complex functions. Representation of function by a set of mutually orthogonal functions, Dirichlet"s conditions, Trigonometric Fourier series and Exponential Fourier series, Spectrum and its significance, Amplitude and Phase spectra, bandwidth of a signal.

UNIT-II

Fourier transform: Fourier transform, Fourier transform of standard signals, properties of Fourier transforms, Fourier transforms involving impulse function, Fourier transform of periodic signals.

UNIT-III

Discrete Time Signals: Sampling of continuous time signals, Sampling theorem, Reconstruction of signal from its samples, effect of under sampling – Aliasing. Elementary sequences- Unit impulse, step, ramp, and exponential sequences, Periodicity of Discrete-time signals, Operations on Discrete-time signals.

Convolution and correlation: Graphical method of convolution, auto correlation and Cross correlation of functions, properties of correlation function, Energy density spectrum, Power density spectrum, Relation between convolution and correlation, Applications of convolution and correlation.

UNIT-IV

Response of LTI systems: Systems, Classification of Systems, Linear time invariant (LTI) system, Transmission of signals through LTI systems, Transfer function of a LTI system, Causality & Stability. Distortion less transmission through LTI system, Bandwidth of systems, relation between bandwidth and rise time.

Discrete Time Systems: Definition, classification, Linear Shift Invariant(LSI) system, Stability, Causality, Linear constant coefficient difference equation, Impulse response, Discrete time Fourier transform, Properties, Transfer function, System analysis using DTFT.

UNIT-V

Laplace Transform: Definition , ROC , Properties , Inverse Laplace transform , The S-plane and BIBO stability , Transfer functions , System response to standard signals.

Z–Transform: Definition, ROC and its properties, analysis of LTI system using Z-transform, The Inverse Z-transform using, Z-transform properties, Unilateral Z- Transform, solution of linear constant coefficient difference equations using Z-transforms.

Text Books:

1. Simon Haykin, Van Veen, and Wiley, "Signals & Systems", 2nd Edition, 2003.
2. Oppenheim AV and Willisky, "Signals and Systems", 2nd Edition, Pearson Ed, 1997.
3. B.P. Lathi, "Principles of Linear systems and signals," Oxford Univ. Press, Second Edition International version, 2009.
4. 4. Tarun Kumar Rawat, "Signals and Systems", Oxford University Press.

Reference Books:

1. Simon Haykin, "Communication Systems", 2nd Edition, Wiley-Eastern, 2003.
2. Luis F. Chaparro, "Signals and Systems using MATLAB," Academic Press, 2011.
3. P. Ramesh Babu, R. Ananda Natarajan, "Signals and Systems", 2nd edition, SciTech Publications, 2006.
4. John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing, Principles, Algorithms ,and Applications", 4 th Edition, PHI, 2007.

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Course Title	Network Theory				B. Tech. ECE III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
2004304	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

To learn network theorems,

To teach application of resonance, transients applied for ac and dc circuits

To study necessary conditions for network functions, various parameters and its relationships.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Analyze RL, RC and RLC for DC transient response.
CO 2	Analyze RL, RC and RLC for AC transient response.
CO 3	Understand the basic concepts of magnetic circuits, resonance and network functions.
CO 4	Analyze two port networks for Z, Y, ABCD, H parameters and its relationship between them.
CO 5	Understand network topology.

UNIT – I

Network topology: Introduction, definitions, formation of incidence matrix, cutest, tie set, loop current method of analysis, crammer's method, driving point and transfer impedance, dual networks, procedure to obtain dual network.

UNIT – II

DC Transient Analysis: Determination of initial conditions – transient response of R-L, R-C & R-L-C circuits for dc–solution method using differential equation and Laplace transforms.

UNIT – III

AC Analysis: Transient response of R-L, R-C and R-L-C series circuits for sinusoidal excitations, solution method using differential equation and Laplace transforms.

Resonance: Series, parallel circuits, concept of half power frequencies, bandwidth and Q factor. Simple problems.

UNIT – IV

Network Synthesis: Causality and Stability, Positive Real Function, Hurwitz Polynomial, Testing Driving Point Immittances, Elementary Synthesis Procedures, Properties of LC Immittances.

UNIT – V

Two port Networks: one port, two port and n-port networks, driving point impedance and admittance, transfer impedance and admittance, voltage and current ratios, impedance parameters, admittance parameters, transmission parameters, hybrid and inverse hybrid parameters, relationship between parameters, conditions for symmetry and reciprocity.

Text Books

1. M.E Van Valkenburg "Network Analysis" –- 3rd edition, PHI, 2015.
2. Hayt and Kimmerly "Engineering circuit analysis", 7th edition, TMH, 2010.
3. N.Sreenivasulu, "Electrical Circuits", Reem publications, 2012.

4.A.Chakrabarti, "Circuit Theory", seventh edition, Dhanapat Rai & Co publications, 2015

Reference Books

1. A. Sudhakar, Shayammohan. S. Pillai "Circuits & Networks" –, 4th Edition –. TMH, 2013.
2. Stanley "Network Analysis with applications", 4th edition, Pearson education, 2004.
3. D. Roy Chowdari "Networks and Systems" — New Age International
4. "Fundamentals of Electrical Networks" by BR Guptha and V.Singhal, S.Chand.

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Course Title	ANALOG CIRCUITS LAB				B. Tech. ECE III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
2004307	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		--	--	3	1.5	40	60	100
					End Exam Duration: 3Hrs		

Course Objectives:

The objective of the course is to verify theoretically and practically all the experiments, analyze the characteristics of BJT, design the oscillators, feedback amplifier circuits, power amplifier circuits and multi-vibrator circuits from the

Course Outcomes: On successful completion of this laboratory course, the students will be able to

CO 1	Verify the characteristics of amplifiers with and without feedback.
CO 2	Observe the output waveforms of different oscillators.
CO 3	Analyze the characteristics of power amplifiers.
CO 4	Design monostable Multivibrator circuit.

List of Experiments:

1. Common Emitter Amplifier
2. Common Source Amplifier
3. Common Drain Amplifier
4. Two Stage RC Coupled Amplifier
5. Cascode amplifier Circuit
6. Darlington Pair Circuit
7. Current Shunt Feedback amplifier Circuit
8. Voltage Series Feedback amplifier Circuit
9. RC Phase shift Oscillator Circuit(using MOSFET)
10. Hartley and Colpitt's Oscillators Circuit
11. Class A power amplifier
12. Class B Complementary symmetry amplifier
13. Design a Monostable Multivibrator
14. The output voltage waveform of Miller Sweep Circuit

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Course Title	PYTHON PROGRAMMING				B. Tech. ECE III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
20SC308	SC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		1	--	2	2	40	60	100
					End Exam Duration: 3Hrs		

Course Objectives:

To write, test, and debug simple Python programs.

To implement Python programs with conditionals and loops.

Use functions for structuring Python programs.

Represent compound data using Python lists, tuples and dictionaries.

Read and write data from/to files in Python

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Demonstrate the functions in Python programming.
CO 2	Illustrate Python programs with conditionals and loops.
CO 3	Test functions for structuring Python programs.
CO 4	Design functions for structuring Python programs.
CO 5	Evaluate compound data using Python lists, tuples, dictionaries.

LIST OF PROGRAMS

1. Compute the GCD of two numbers.
2. Find the square root of a number (Newton's method)
3. Exponentiation (power of a number)
4. Find the maximum of a list of numbers
5. Linear search and Binary search
6. Selection sort, Insertion sort
7. Merge sort
8. First n prime numbers
9. Multiply matrices
10. Programs that take command line arguments (word count)
11. Find the most frequent words in a text read from a file
12. Simulate elliptical orbits in Pygame
13. Simulate bouncing ball using Pygame

PLATFORM NEEDED

Python 3 interpreter for Windows/Linux

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Course Title	LINEAR AND DIGITAL IC APPLICATIONS				B. Tech. ECE IV Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
2004405	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

To give introduction to Op-Amps.

To study about Timers and PLLs.

To learn the applications of Op-Amps.

To introduce Verilog and its language elements to design digital systems

Make students familiar with design of different combinational and sequential digital circuits.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the operation and characteristics of OP-AMPs, CMOS, Bipolar logic families and its interfacing.
CO 2	Applying basic equations and compute the parameters of Multivibrators.
CO 3	Analyze the circuits with OP-AMPs, 555timers.
CO 4	Apply the concepts of Verilog HDL for modeling and simulation of digital logic circuits.
CO 5	Design op-amp, 555timer circuits and logic circuits.

UNIT-I

OP-AMP AND ITS CHARACTERISTICS: Differential Amplifier- DC and AC analysis of Dual input Balanced output Configuration, Properties of other differential amplifier configuration (Dual Input Unbalanced Output, Single Ended Input Balanced/ Unbalanced Output), Integrated circuits - types, classification, package types and temperature ranges, power supplies, OP-Amp Block diagram, ideal and practical OP-Amp specifications, DC and AC characteristics, Frequency Compensation. 741 OP-Amp and its features, Inverting and non-inverting amplifier.

UNIT-II

OP-AMP APPLICATIONS: Summer, Subtractor, Integrator and differentiator, instrumentation amplifier, AC amplifier, V-I, I-V converters, comparators, Multivibrators, Triangular and square wave generators, precision rectifiers. Introduction to Analog Active Filters, Design and analysis of first order and second order LPF and HPF.

UNIT-III

TIMERS AND PHASE LOCKED LOOPS: Introduction to 555 Timer, Functional diagram, Monostable and Astable operations, Schmitt Trigger, PLL-Introduction, Block schematic, principles and description of individual blocks, IC 565 and PLL applications.

UNIT–IV

CMOS Logic and Interfacing: CMOS logic, CMOS NAND and NOR gates, CMOS AOI and OAI gates, CMOS steady state and dynamic electrical behavior, CMOS logic families, CMOS/TTL interfacing, low voltage CMOS logic and interfacing. CMOS transmission gates, Bi- CMOS. Familiarity with standard 74XX and CMOS 40XX series-ICs – Specifications and Applications.

UNIT–V

Verilog HDL AND DESIGN EXAMPLES: HDL based Design flow, **Verilog** Program Structure, Nets, Variables and Constants, Vectors and Operators, Arrays, Logical Operators and Expressions. **Verilog** modeling styles: Structural design elements, data flow design elements, behavioral design elements (procedural code). Design using basic gates, Decoders, Encoders, Multiplexers, Adders, Subtractors, SSI Latches and Flip-Flops, Counters and Shift Registers. **Verilog** Modules for the above ICs.

Text Books:

1. Ramakanth A. Gayakwad, "Op-Amps & Linear ICs", 4th edition, PHI, 1987.
2. John F. Wakerly, "Digital Design Principles & Practices" PHI/Pearson Education Asia, 4th Edition,2008.
3. J. Bhasker, "A Verilog HDL Primer", Star Galaxy Publishing; 3rd edition (January 31, 2005)
4. Verilog HDL – Samir Palnitkar, 2nd Edition, Pearson Education, 2009.

References:

1. D. Roy Chowdhury, "Linear Integrated Circuits", New Age International (P) Ltd, 2nd Edition, 2003.
2. James M.Fiore, "Operational Amplifiers & Linear integrated circuits & applications", Cengage 2009.
3. William D Stanley, "Operational Amplifiers with Linear Integrated Circuits", Pearson education India, 2002.
4. Fundamentals of Digital Logic with Verilog Design – Stephen Brown, Zvonko Vranesic, TMH, 3rd Edition, 2014

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Course Title	LINEAR AND DIGITAL IC APPLICATIONS LAB				B. Tech. ECE IV Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
2004406	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		--	--	3	1.5	40	60	100
					End Exam Duration: 3Hrs		

Course Objectives:

To verify various op-amp applications.

To verify the applications of different ICs.

To write Verilog HDL programs for different logic circuits.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Demonstrate the circuits with analog IC's (741, 555, 78XX/79XX, 723).
CO 2	Apply IC's (741, 555, 78XX/79XX, 723) in electronic applications.
CO 3	Design a digital system with Verilog to meet required specifications.
CO 4	Test the functionality of system design with Verilog Test Benches.
CO 5	Test the results of designed digital system using FPGA.

Part A: Analog IC Application Lab:

1. OP AMP Applications – Adder, Subtractor, Comparator Circuits.
2. Active Filter Applications – LPF, HPF (first order).
3. Function Generator using OP AMPs.
4. IC 555 Timer – Monostable and Astable Operation Circuit.
5. IC 566 – VCO Applications.
6. Voltage Regulator using IC 723.
7. 4 bit DAC using OP AMP.
8. Precision Diodes.

Part B: Digital IC Applications:

(Simulate the internal structure of the following Digital IC's using Verilog HDL)

1. Logic Gates- 74XX.
2. Half Adder, Half Subtractor, Full Adder, Full Subtractor & Ripple Carry Adder. 3. 3-8 Decoder -74138 & 8-3 Encoder- 74X148.
4. 8 x 1 Multiplexer -74X151 and 2x4 Demultiplexer-74X155.
5. 4 bit Comparator-74X85.
6. D Flip-Flop 74X74.
7. JK Flip-Flop 74X109.
8. Decade counter-74X90.

Software Required -- Xilinx Vivado

Hardware Required -- FPGA Trainer Kits

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Course Title	MICROPROCESSORS AND MICROCONTROLLERS LAB				B. Tech. ECE IV Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
2004407	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		--	--	3	1.5	40	60	100
						End Exam Duration: 3Hrs		

Course Objectives:

To write 8086microprocessor and 8051 microcontroller programs for various operations

Learning interfacing of processor with various Peripherals.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Develop algorithm and assembly language programs to solve problems.
CO 2	Analyze abstract problems and apply a combination of hardware and software to address the problem.
CO 3	Choosing an appropriate algorithm, program and peripheral for the application.
CO 4	Design the microprocessor based system to solve real time problems.

General Programs

1. Addition and Subtraction of two 8- bit/16 bit numbers, Multiplication of two 8-bit & two 16-bit numbers, Division of 16-bit by 8-bit and 32-bitby 16-bit number
2. Addition and Subtraction of 6 data bytes with 6-data bytes of another location.
3. Check the given Number is even or odd, Counting of 0's and 1's in a given data, Check the given number is logical palindrome or not.
4. Finding the maximum and minimum numbers in a given string of data.
5. Sorting the given numbers in ascending and descending order.
6. Finding the Factorial and Generating Fibonacci Series.
7. Conversion of BCD to hexadecimal number, Multiplication of two 3x3 matrices.
8. Addition, Subtraction, Multiplication, Division using Microcontroller.

Interfacing

1. Dual DAC interface (waveform generation).
2. Stepper motor control.
3. Display of flags using logic controller.
4. Traffic light controller.

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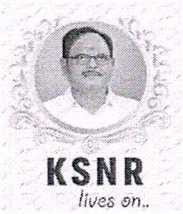

Department of ECE
M.Tech Embedded Systems and VLSI
Course Structure

Semester-I									
S.No	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	1884101	RTL Simulation and Synthesis with PLDs	PC	3	0	0	40	60	3
2.	1884102	Microcontrollers and Programmable Digital Signal Processors	PC	3	0	0	40	60	3
3.	1884103	Research methodology and IPR	PC	2	0	0	40	60	2
4.	1884104 1884105 1884106 1884107	1. Parallel Processing 2. Digital Signal and Image Processing 3. VLSI signal processing 4. Design for testability	PE	3	0	0	40	60	3
5.	1884108 1884109 1884110 1884111	1. Programming Languages for Embedded Systems. 2. Micro-Electro Mechanical systems. 3. CAD of Digital System 4. CPLD, FPGA architectures and applications.	PE	3	0	0	40	60	3
6.	1884112	RTL Simulation and Synthesis with PLDs Lab	PC	0	0	4	40	60	2
7.	1884113	Microcontrollers and Programmable Digital Signal Processors Lab	PC	0	0	4	40	60	2
8.	1870A02	Disaster Management	AC				40		0
									18

Semester-II									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	1884201	Analog and Digital CMOS VLSI Design	PC	3	0	0	40	60	3
2.	1884202	Real Time Operating Systems	PC	3	0	0	40	60	3
3.	1884203 1884204 1884205 1884206	1. Memory Architectures 2. Advanced Computer Architecture 3. SoC Design 4. Low power VLSI Design	PE	3	0	0	40	60	3
4.	1884207 1884208 1884209 1884210	1. Communication Buses and Interfaces 2. Network Security and Cryptography 3. Physical design automation 4. Nanoelectronics	PE	3	0	0	40	60	3
5.	1884211	Analog and Digital CMOS VLSI Design Lab	PC	0	0	4	40	60	2
6.	1884212	Real Time Operating Systems Lab	PC	0	0	4	40	60	2
7.	1884213	Mini Project	PC	0	0	4	100	0	2
8.	1870A01	English for Research paper writing	AC				40		0
									18

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Semester-III									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	1884301 1884302 1884303 1884304	1. IOT and its Applications 2. Hardware Software co-design 3.Artificial Intelligence 4. RFIC Design	PE	3	0	0	40	60	3
2.	1871305 1871306 1871307 1871308 1871309 1871310	1. business Analytics 2. Industrial Safety 3. Operations Research 4. Cost Management of EngineeringProjects 5. Composite Materials 6. Waste to Energy	OE	3	0	0	40	60	3
3.	1884311	Dissertation Phase -I	Major Project	0	0	20	100	0	10
									16

Semester-IV									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	1884401	Dissertation Phase II	Major Project	0	0	32	50	50	Dissertation Phase II
									16

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Course Title	RTL SIMULATION AND SYNTHESIS WITH PLDS				M. Tech. ES &VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884101	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To introduce Verilog HDL for the design and functionality verification of a digital circuit.
- To understand the design of data path and control circuits for sequential machines
- To introduce the concept of realizing a digital circuit using PLDs

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the Static Timing Analysis and clock issues in digital circuits
CO 2	Appreciate the analysis of finite state machine of a controlling circuit
CO 3	Develop the Verilog HDL to design a digital circuit.
CO 4	Verify the functionality of the digital designs using PLDs.

UNIT-I:

Verilog HDL: Importance of HDLs, Lexical Conventions of Verilog HDL Gate level modeling: Built in primitive gates, switches, gate delays Data flow modeling: Continuous and implicit continuous assignment, delays Behavioural modeling: Procedural constructs, Control and repetition Statements,delays, function and tasks.

UNIT-II:

Digital Design: Design of BCD Adder, State graphs for control circuits, shift and add multiplier, Binary divider.FSM and SM Charts: Finite state diagram, Implementation of sequence detector using FSM, State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier.

UNIT-III:

ASIC Design Flow: Simulation, simulation types, Synthesis, synthesis methodologies, translation, mapping, optimization, Floor planning, Placement, routing, Clock tree synthesis, Physical verification.

UNIT-IV:

Static Timing Analysis: Timing paths, Meta-stability, Clock issues, Need and design strategies for multi- clock domain designs, setup and hold time Violations, steps to remove Setup and hold time violations.

UNIT-V:

Digital Design using PLD"s: ROM, PLA, PAL- Registered PAL"s, Configurable PAL"s, And GAL.CPLDs: Features, programming and applications using complex programmable logic devices. FPGAs: FieldProgrammable gate arrays Logic blocks, routing architecture, design flow.

TEXT BOOKS:

1. Samir Palnitkar Verilog HDL,A Guide to "Digital Design and Synthesis", 2nd Edition, 2003
2. Charles H. Roth "Fundamentals of Logic Design" , 5th Edition. Cengage Learning, 2010.
3. Bhasker J Verilog HDL Synthesis A Practical Primer, 1st edition, 1998
4. Modern Digital Electronics P Jain, 3rd Edition, TMH, 2003.

REFERENCES:

1. Donald D Givone, "Digital principles and Design", TMH, 2016
2. Bob Zeidman, "Designing with FPGAs & CPLDs", CMP Books, 2002.
3. Richard S. Sandige, "Modern Digital Design", MGH, International Editions, 1990
4. Data Sheets for CPLD & FPGA architectures, 1996.

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Course Title	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS				M. Tech. ES&VLSI I Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
		L	T	P	C	Continuous Internal Assessment	End Exams	Total
1884102	PC	3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand, compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
- To be able to identify and characterize architecture of Programmable DSP Processors
- To develop small applications by utilizing the ARM processor core and DSP processor based platform.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
CO 2	Identify and characterize architecture of Programmable DSP Processors
CO 3	Develop small applications by utilizing the ARM processor core and DSP processor based platform.

UNIT-I

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT-II

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration.

UNIT-III

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT-IV

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.

UNIT-V

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for application development for digital signal processing.

TEXT BOOKS:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition.
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication
4. ARM System Developer's Guide-Designing and Optimizing system software, Andrew N.Sloss, Dominic Symes, Chris Wright, Elsevier, 2008.

REFERENCES:

1. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
2. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
3. Technical references and user manuals on www.arm.com.

4. Steve Furbur, ARM System onchip Architecture, 2nd Edition, Addison Wesley, 2000.

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Course Title	RESEARCH METHODOLOGY AND IPR				M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884103	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		2	0	--	2	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand research problem formulation.
- To Analyze research related information
- To Follow research ethics
- To understanding that when IPR would take such important place in growth of individuals & nation,it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- To understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about,economic growth and social benefits.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand research problem formulation.
CO 2	Analyze research related information
CO 3	Follow research ethics
CO 4	Apply Patent Rights in filing.
CO 5	Describe new developments in IPR.

UNIT I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

UNIT II

Effective literature studies approaches, analysis Plagiarism and Research ethics. Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT III

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT IV

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and

databases. Geographical Indications.

UNIT V

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies,IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science& engineering students"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd , 2007.

REFERENCES:

1. Mayall, "Industrial Design", McGraw Hill, 1992.
2. Niebel, "Product Design", McGraw Hill, 1974.
3. Asimov, "Introduction to Design", Prentice Hall, 1962.
4. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
5. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

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Course Title	PARALLEL PROCESSING					M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
1884104	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To overview of the architectures and communication networks employed in parallel computers.
- The course covers the foundations for development of efficient parallel algorithms, including examples from relatively simple numerical problems, sorting, and graph problems.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand parallel processing and pipelining techniques.
CO 2	Identify limitations of different architectures of computer
CO 3	Analysis quantitatively the performance parameters for different architectures
CO 4	Investigate issues related to compilers and instruction set based on type of architectures
CO 5	Develop parallel programming techniques.

UNIT I

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

UNIT II

Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

UNIT III

VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

UNIT IV

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions

UNIT V

Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems Customizing applications on parallel processing platforms

TEXT BOOKS:

1. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition
2. Kai Hwang, "Advanced Computer Architecture", TMH
3. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.
4. David A Patterson and John L Hennessy, "Computer Organization and Design: The Hardware/Software Interface", Morgan Kaufmann; 4th edition.

REFERENCES:

1. William Stallings, "Computer Organization and Architecture, Designing for performance "Prentice Hall, Sixth edition
2. Kai Hwang, ZhiweiXu, "Scalable Parallel Computing", MGH
3. David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan
4. Joseph D. Dumas II, "Computer Architecture: Fundamentals and principles of Computer Design", BS Publication.

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Course Title	DIGITAL SIGNAL AND IMAGE PROCESSING				M. Tech. ES & VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884105	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	0	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To study the discrete time signals and system in various domains
- To learn the concepts of design of digital filtering
- To study different image enhancement, Restoration and compression techniques
- To understand image segmentation algorithms

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Analyze discrete-time signals and systems in various domains(i.e. Time, Z and Fourier)
CO 2	Design the digital filters (both IIR and FIR)from the given specifications
CO 3	Analyzethequantizationeffectsindigitalfiltersandunderstandthebasicsofimagesampling, quantization and image transforms.
CO 4	Understand the concepts of image enhancement, image restoration, image segmentation and Color Image processing
CO 5	Analyze various image compression techniques

UNIT I

Review of Discrete Time signals and systems, Characterization in time, Z and Fourier domain, Fast Fourier Transform using Decimation In Time (DIT) and Decimation In Frequency (DIF) Algorithms.

UNIT II

IIR Digital Filters: Introduction, Analog filter approximations–Butterworth and Chebyshev, Design of IIR Digital filters from analog filters using Impulse Invariance, Bilinear Transformation methods.
FIR Digital Filters: Introduction, Design of FIR Digital Filters using Window Techniques, Frequency Sampling technique, Comparison of IIR &FIR filters.

UNIT III

Analysis Of Finite Word length Effects: The Quantization Process and Errors, Quantization of Fixed-Point Numbers, Quantization of Floating- Point Numbers ,Analysis of Coefficient Quantization effects.
Introduction To Digital Image Processing: Introduction, components in image processing system, Applications of Digital image processing, Image sensing and acquisition, Image sampling, Quantization, Basic Relationships between pixels, ImageTransforms:2D-DFT, DCT, Haar Transform.

UNIT IV

Image Enhancement: Intensity transformation functions, histogram processing, fundamentals of spatial filtering, smoothing spatial filters, sharpening spatial filters, the basics of filtering in the frequency domain, image smoothing using frequency domain filters, Image Sharpening using frequency domain filters ,Selective filtering.

Image Restoration: Introduction, restoration in the presence of noise only-Spatial Filtering, Periodic Noise Reduction by frequency domain filtering, Linear, Position –Invariant Degradations, Estimating the degradation function, Inverse filtering, Minimum mean square error (Wiener) filtering.
Image Segmentation: Fundamentals, point, line, edge detection, thresholding, and region based segmentation.

UNIT V

Image Compression: Fundamentals, Basic compression methods: Huffman coding, Arithmetic coding, Run-Length coding, Block Transform coding, Predictive coding, Wavelet coding.

Color Image Processing: color fundamentals, color models, pseudo color image processing, basics of full color image processing, color transformations, smoothing and sharpening. Image segmentation based on color, noise in color images, color image compression.

TEXT BOOKS:

1. JohnG.Proakis,DimitrisG.Manolakis,"DigitalSignalProcessing",Principles,Algorithms,andApplications,PearsonEducation/PHI,2007.
2. S.K.Mitra."DigitalSignalProcessing–AComputerbasedApproach",TMH,3rdEdition,2006
3. RafaelC.Gonzalez and Richard E.Woods,"Digital Image Processing", PearsonEducation,2011.
4. S.Jayaraman,Esakkirajan,Veerakumar,"DigitalImageProcessing",McGrawHillPublishers,2009

REFERENCES:

1. Andreas Antoniou,"Digital Signal Processing", TATAMcGrawHill, 2006
2. MHHayes, DigitalSignalProcessing, Schaum''sOutlines, TATAMc-GrawHill, 2007.
3. AnilK.Jain,"Fundamentals of Digital Image Processing" ,PrenticeHall ofIndia,2012.
4. Somka,Hlavac Boyle,"Digital image Processing and computer vision"Cengage learning (Indian edition,2008)

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Course Title	VLSI SIGNAL PROCESSING					M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
1884106	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To understand the static, small signal and large signal modeling of MOS Transistor.
- To understand the DSP architectures.
- To understand the operation of design aspects of processors.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Ability to modify the existing or new DSP architectures suitable for VLSI.
CO 2	Understand the concepts of folding and unfolding algorithms and applications.
CO 3	Analyze to implement fast convolution algorithms.
CO 4	Develop Low power design aspects of processors for signal processing and wireless applications.

UNIT I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT II

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems

Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT V

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design .Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

Text Books:

1. Keshab K. Parthi[A1] , "VLSI Digital signal processing" systems, design and implementation[A2] , Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, "Analog VLSI signal and information processing", McGraw Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.

4. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits – Analysis and Design, TMH,2011.

References:

1. A. P. Chandrasekaran and R. W. Broadersen, "Low power digital CMOS design", Kluwer,1995

2. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

3. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.

4. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System Perspective" CRC Press,2011

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Course Title	DESIGN FOR TESTABILITY				M. Tech. ES &VLSI		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884107	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To analyze the digital circuits with the presence of faults.
- To generate the test patterns.
- To understand the concept of controllability and observability.
- To determine the built in self test.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Design digital circuits including various levels of modeling and different approaches for simulation.
CO 2	Analyze the digital circuits with the presence of faults and evaluation of given test set for fault coverage.
CO 3	Create test patterns for detecting single stuck faults in combinational and sequential circuits.
CO 4	Explain controllability and observability and schemes for introducing testability into digital circuits which will make circuits more testable with ease and improve fault coverage.
CO 5	Determine built in self test (BIST) and different approaches for introducing BIST into logic circuits memories and embedded cores.

UNIT I

Introduction to Test and Design for Testability (DFT) Fundamentals. Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of modeling. Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

UNIT II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits.

UNIT III

Testing for single stuck faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT IV

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT – V

Built-in self-test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level. Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

TEXT BOOKS:

1. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 2001.
2. Alfred Crouch., "Design for Test for Digital ICs & Embedded Core Systems", Prentice Hall.
3. Robert J. Feugate, Jr., Steven M. Mentyn, "Introduction to VLSI Testing", Prentice Hall, Englehood Cliffs, 1998.
4. M.L. Bushnell, V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits" Kluwer Academic Publishers.

REFERENCES:

1. M. Abramovici, M. A. Breuer and A.D Friedman, "Digital Systems and Testable Design", Jaico Publishing House.
2. P.K. Lala, "Digital Circuits Testing and Testability", Academic Press.
3. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.
4. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System
5. Perspective" CRC Press,2011

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Course Title	PROGRAMMING LANGUAGES FOR	M. Tech. ES &VLSI I Sem

	EMBEDDED SYSTEM							
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
1884108	**PE**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**			

Course Objectives:

- To explore the difference between general purpose programming languages and Embedded Programming Language.
- To provide case studies for programming in embedded systems.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Expected to learn the basics of Embedded C with reference to 8051.
CO 2	Understand how to handle control and data pins at hardware level.
CO 3	Capable of introducing into objective nature of Embedded C.
CO 4	Understand the specifications of real time embedded programming with case studies

UNIT I

Programming Embedded Systems in C Introduction, What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family

Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT II

Reading Switches Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT III

Adding Structure to your Code Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT IV

Meeting Real-Time Constraints Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT V

Case Study: Intruder Alarm System Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

Text Books:

1. 1. Michael J. Pont "Embedded C", A Pearson Education
2. Embedded / Real-Time Systems: Concepts, Design and Programming Black Book by Dr. K.V.K.K. Prasad, Dreamtech Publications.
3. Daniel D. Gajski, Frank Vahid, Sanjiv Narayan, Jie Gong, "Specification and Design of Embedded Systems", Prentice Hall, 1994.
4. Abraham Silberschatz and Peter B Galvin, "Operating System Concepts", Addison Wesley, 1995.

References:

1. Introduction to embedded systems - by Raj Kamal, TMH, 2002.
2. An Embedded Software primer, David E.Simon, 1stedition, Addison Wesley professional, 2007.
3. Peter Marwedel, "Embedded System Design", Springer; 1st edition.
4. Jonathan W. Valvano, "Introduction to Embedded Systems", Cengage Publishing.

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